TPS7A05 1-µA Ultralow I_Q, 200-mA, Low-Dropout Regulator in a Small-Size Package

1 Features

- Ultralow I_Q: 1 µA (typ), 3 µA (max)
  - I_{GND}: 6 µA (typ) at 200 mA
- Excellent transient response
- Packages:
  - 1.0-mm × 1.0-mm X2SON (4)
  - 0.65-mm × 0.65-mm DSBGA (4)
  - SOT-23 (5)
  - SOT-23 (3) (preview)
- Input voltage range: 1.4 V to 5.5 V
- Output accuracy: 1% typical, 3% maximum
- Available in fixed-output voltage:
  - 0.8 V to 3.3 V
- Very low dropout:
  - 235 mV (max) at 200 mA (3.3 V_{OUT})
- Active output discharge
- Foldback current limit
- Stable with a 0.47-µF or larger capacitor

2 Applications

- Wearable electronics
- Ultrabooks, tablets, E-readers
- Always-on power supplies
- Set-top boxes
- Gaming controllers, remote controls, toys, drones
- Wireless handsets and smart phones
- Portable and battery-powered equipment

3 Description

The TPS7A05 is an ultra-small, low quiescent current low-dropout regulator (LDO) that can source 200 mA with excellent transient performance. This device has an output range of 0.8 V to 3.3 V with a typical 1% accuracy.

The TPS7A05, with ultralow I_Q (1 µA), consumes very-low quiescent current for extending battery life in battery-powered applications. The device can be operated from rechargeable Li-Ion batteries, Li-primary battery chemistries such as Li-SOCl2, Li-MnO2, as well as two- or three-cell alkaline batteries.

The TPS7A05 is available with an active pulldown circuit to quickly discharge the output when disabled.

The TPS7A05 is fully specified for T_J = –40°C to +125°C operation, and is available in standard X2SON (DQN), SOT-23 (DBV and DBZ), and DSBGA (YKA) packages.

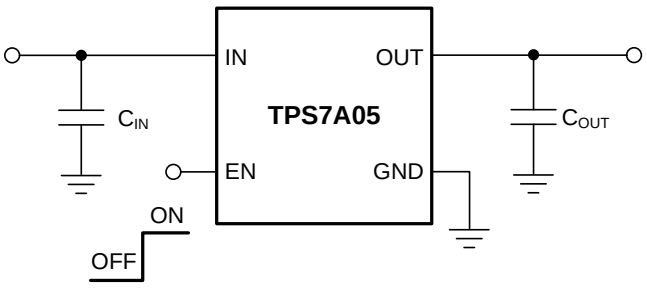
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A05	X2SON (4)	1.00 mm × 1.00 mm
	DSBGA (4)	0.65 mm × 0.65 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	SOT-23 (3)(2)	2.90 mm x 1.60 mm

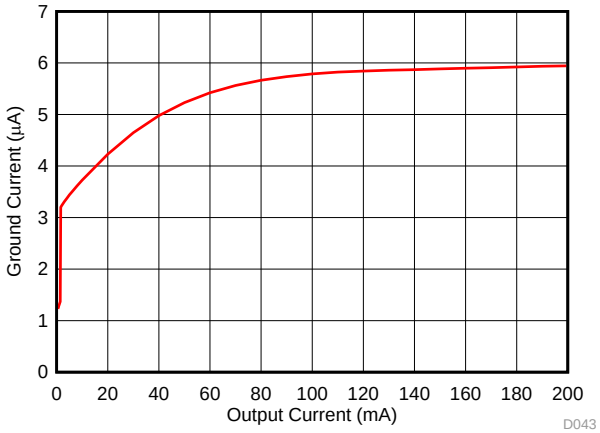
(1) For all available packages, see the package option addendum at the end of the data sheet.

(2) Preview package.

Typical Application Circuit



Ground Current vs Output Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision B (August 2018) to Revision C — **Page**

- Added DBZ package to document as APL release ... 1

Changes from Revision A (May 2018) to Revision B — **Page**

- Changed *1-mm × 1-mm* to *Small-Size* in document title ... 1
- Changed YKA (DSBGA) package status to production data ... 1
- Added Accuracy for 1.825 V in *Electrical Characteristics* table ... 6
- Changed Output current limit in *Electrical Characteristics* table ... 6
- Added Output current limit for +85°C in *Electrical Characteristics* table ... 6
- Changed Short-circuit current limit in *Electrical Characteristics* table ... 6
- Added Dropout voltage for 1.825 V in *Electrical Characteristics* table ... 6
- Changed y-axis scaling and added conditions for I_{OUT} *Transient 0 mA to 100 mA* figure ... 8
- Changed y-axis scaling and added conditions for I_{OUT} *Transient 0 mA to 200 mA* figure ... 9
- Added I_{OUT} *Transient 0 mA to 50 mA* figure to I_{OUT} *Transient 3 µA to 3 mA* figure ... 9
- Added slew rate condition to V_{IN} *Transient* figures (I_{OUT} = 100 mA and I_{OUT} = 200 mA) ... 10
- Added V_{IN} *Transient* figures (I_{OUT} = 150 mA and I_{OUT} = 20 mA) ... 11
- Added V_{IN} condition to *PSRR vs Frequency and* I_{OUT} figure (V_{OUT} = 1.8 V) ... 14

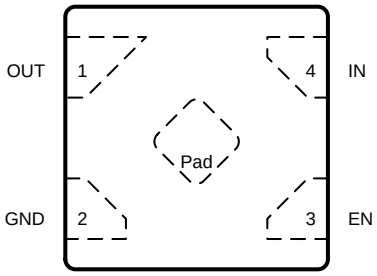
Changes from Original (February 2018) to Revision A — **Page**

- Released to production ... 1

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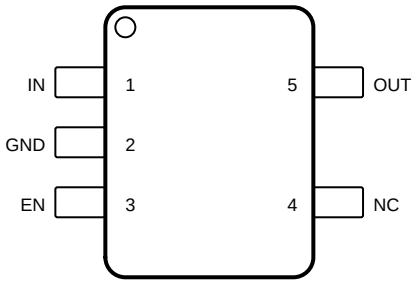
5 Pin Configuration and Functions

DQN Package
1-mm × 1-mm, 4-Pin X2SON
Top View



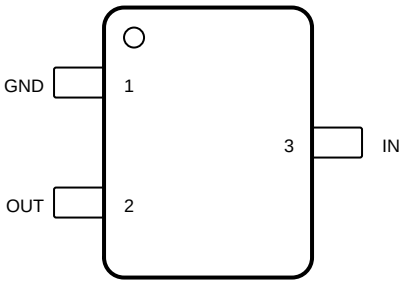
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DBV Package
5-Pin SOT-23
Top View



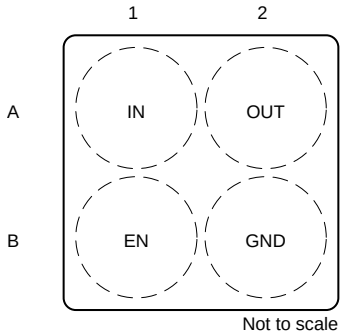
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DBZ Package (Preview)
3-Pin SOT-23
Top View



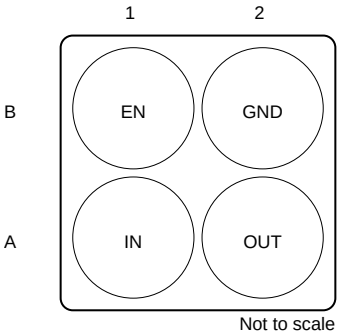
Not to scale

YKA Package
4-Pin DSBGA, 0.35-mm Pitch
Top View



Not to scale

YKA Package
4-Pin DSBGA, 0.35-mm Pitch
Bottom View



Not to scale

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Pin Functions

PIN					I/O	DESCRIPTION
NAME	DQN	DBV	DBZ	YKA		
IN	4	1	3	A1	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to input of the device as possible.
EN	3	3	—	B1	Input	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN. V_{EN} must not exceed V_{IN}.
GND	2	2	1	B2	—	Ground pin. This pin must be connected to ground on the board.
OUT	1	5	2	A2	Output	Regulated output pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground. Follow the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to output of the device as possible.
NC	—	4	—	—	—	No connect pin. This pin is not internally connected. Connect to ground or leave floating.
Thermal pad	Pad	—	—	—	—	Connect the thermal pad to a large-area ground plane. This pad is not an electrical connection to the device ground.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	IN	–0.3	6.0	V
	EN	–0.3	V_{IN} + 0.3	
	OUT	–0.3	V_{IN} + 0.3 or 3.6(3)	
Current	Maximum output current	Internally limited		A
Temperature	Operating junction temperature, T_J	–40	125	°C
	Storage temperature, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages with respect to GND.
(3) V_{IN} + 0.3 V or 3.6 V (whichever is smaller)

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	1.4		5.5	V
V_{EN}	Enable supply voltage	0		V_{IN}	V
V_{OUT}	Nominal output voltage range	0.8		3.3	V
I_{OUT}	Output current(1)	0		200	mA
C_{IN}	Input capacitor		1		µF
C_{OUT}	Output capacitor	0.47	1	22	µF
T_J	Operating junction temperature	–40		125	°C

(1) Output current of 10 µA minimum required to meet output voltage accuracy specification.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A05				UNIT
		DBZ (SOT-23)	DBV (SOT-23)	DQN (X2SON)	YKA (DSBGA)	
		3 PINS	5 PINS	4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	267.3	185.6	144.1	198.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	103.5	104.3	137.9	2.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	98.0	54.5	83.5	66.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.2	31.0	5.3	0.9	°C/W
Y_{JB}	Junction-to-board characterization parameter	97.4	54.5	83.8	76.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	71.8	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

specified at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 1.4 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Nominal accuracy(1)	V_{OUT} ≥ 1.0 V, T_J = 25°C		–1%		1%	
		V_{OUT} < 1.0 V, T_J = 25°C		–10		10	mV
	Accuracy over temperature(1)	V_{OUT} ≥ 1.0 V, T_J = –40°C to +85°C		–2%		2%	
		V_{OUT} ≥ 1.0 V		–3%		3%	
		V_{OUT} < 1.0 V, T_J = –40°C to +85°C		–20		20	mV
		V_{OUT} < 1.0 V		–30		30	
		V_{OUT} = 1.825 V, T_J = +10°C to +45°C, I_{OUT} = 100 µA		–0.9%		0.9%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V(2), T_J = –40°C to +85°C			5	16.5	mV
		$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V(2)				18	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation(3)	100 µA ≤ I_{OUT} ≤ 200 mA, V_{IN} = $V_{OUT(nom)}$ + $V_{DO(max)}$ + 0.1 V, T_J = –40°C to +85°C			20	43	mV
		100 µA ≤ I_{OUT} ≤ 200 mA, V_{IN} = $V_{OUT(nom)}$ + $V_{DO(max)}$ + 0.1 V				55	mV
I_{GND}	Ground current	T_J = 25°C, I_{OUT} = 1 µA		0.6	1	1.3	µA
		I_{OUT} = 1 µA, T_J = –40°C to +85°C				2	
		I_{OUT} = 1 µA				3	
I_{SHDN}	Shutdown current	V_{EN} = 0.4 V, 1.4 V ≤ V_{IN} ≤ 5.5 V, T_J = 25°C			100	300	nA
I_{CL}	Output current limit	V_{OUT} = 90% × $V_{OUT(nom)}$, V_{IN} = $V_{OUT(nom)}$ + $V_{DO(max)}$ + 0.5 V		210	450	700	mA
I_{CL}	Output current limit	V_{OUT} = 90% × $V_{OUT(nom)}$, V_{IN} = $V_{OUT(nom)}$ + $V_{DO(max)}$ + 0.5 V, T_J = 0°C to +85°C		250	450	700	mA
I_{SC}	Short-circuit current limit	V_{OUT} = 0 V			65	150	mA
V_{DO}	Dropout voltage(4)	I_{OUT} = 200 mA, T_J = –40°C to +85°C	0.8 V ≤ V_{OUT} < 1.0 V			915	mV
			1.0 V ≤ V_{OUT} < 1.2 V			758	
			1.2 V ≤ V_{OUT} < 1.5 V			609	
			1.5 V ≤ V_{OUT} < 1.8 V			469	
			1.8 V ≤ V_{OUT} < 2.5 V			341	
			2.5 V ≤ V_{OUT} < 3.3 V			275	
			V_{OUT} = 3.3 V			212	
		I_{OUT} = 200 mA	0.8 V ≤ V_{OUT} < 1.0 V			1004	
			1.0 V ≤ V_{OUT} < 1.2 V			837	
			1.2 V ≤ V_{OUT} < 1.5 V			679	
			1.5 V ≤ V_{OUT} < 1.8 V			525	
			1.8 V ≤ V_{OUT} < 2.5 V			382	
			2.5 V ≤ V_{OUT} < 3.3 V			308	
			V_{OUT} = 3.3 V			235	
		I_{OUT} = 100 µA, T_J = +10°C to +45°C	V_{OUT} = 1.825 V			20	mV

(1) I_{OUT} ≥ 10 µA required to meet accuracy specifications.
(2) V_{IN} = 1.4 V for V_{OUT} ≤ 0.9 V.
(3) Load Regulation is normalized to the output voltage at I_{OUT} = 1 mA.
(4) Dropout is measured by ramping V_{IN} down until V_{OUT} = $V_{OUT(nom)}$ – 5%.

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Electrical Characteristics (continued)

specified at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 1.4 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power-supply rejection ratio	f = 1 kHz, I_{OUT} = 30 mA		40		dB
		f = 500 kHz, I_{OUT} = 30 mA		30		
		f = 1 MHz, I_{OUT} = 30 mA		40		
V_N	Output voltage noise	BW = 10 Hz to 100 kHz, V_{OUT} = 1.2 V, I_{OUT} = 30 mA		180		μV_{RMS}
V_{UVLO}	UVLO threshold	V_{IN} rising	1.21	1.3	1.37	V
$V_{UVLO(HYST)}$	UVLO hysteresis	V_{IN} falling		40		mV
V_{UVLO}	UVLO threshold	V_{IN} falling	1.17		1.33	V
$V_{EN(HI)}$	EN pin logic high voltage		0.9			V
$V_{EN(LO)}$	EN pin logic low voltage				0.4	V
I_{EN}	EN pin current	V_{EN} = V_{IN} = 5.5 V		10		nA
$R_{PULLDOWN}$	Pulldown resistor	V_{IN} = 3.3 V, P version only		120		Ω
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		

6.6 Switching Characteristics

specified at T_J = –40 to +125°C, V_{IN} = $V_{OUT(nom)}$ + $V_{DO(max)}$ + 0.5 V, I_{OUT} = 10 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Start-up time(1)	From EN assertion to V_{OUT} = 95% × $V_{OUT(nom)}$, V_{OUT} = 1.8 V		1.5	2.8	ms

(1) See the *Special Considerations When Ramping Down IN and Enable* section for details on minimum ramp down rates to ensure specified start-up time.

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6.7 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

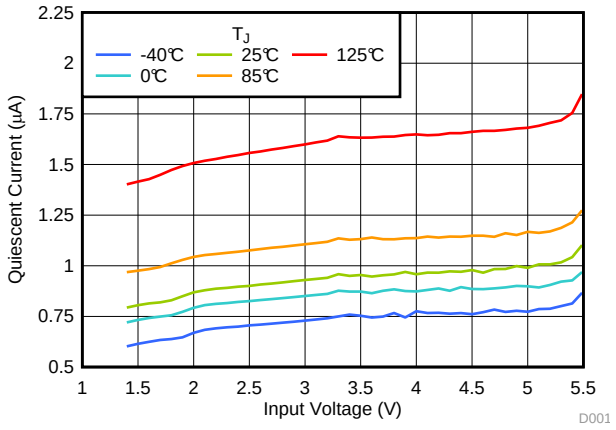


Figure 1. I_Q vs V_{IN} and Temperature

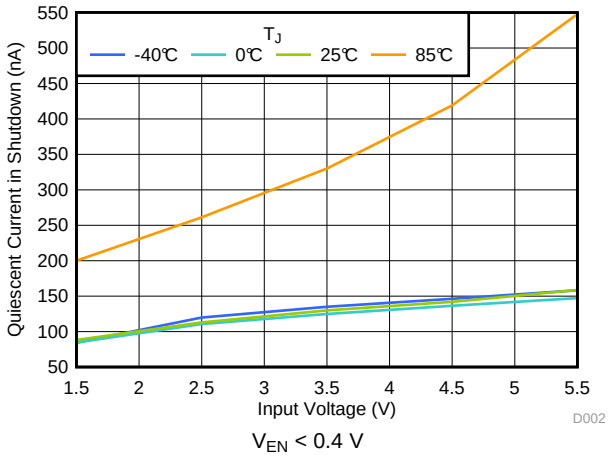


Figure 2. I_{SHDN} vs V_{IN} and Temperature

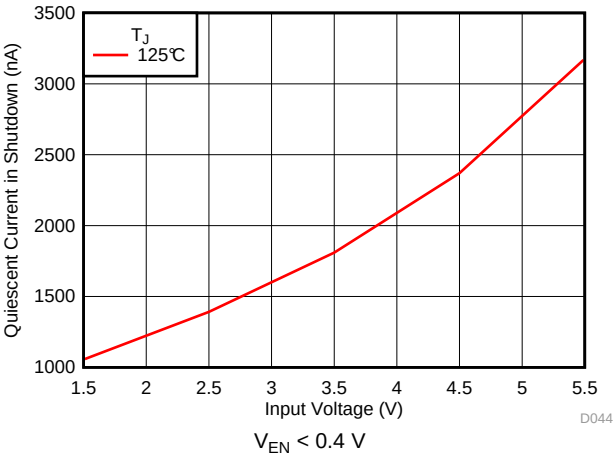


Figure 3. I_{SHDN} vs V_{IN} and Temperature

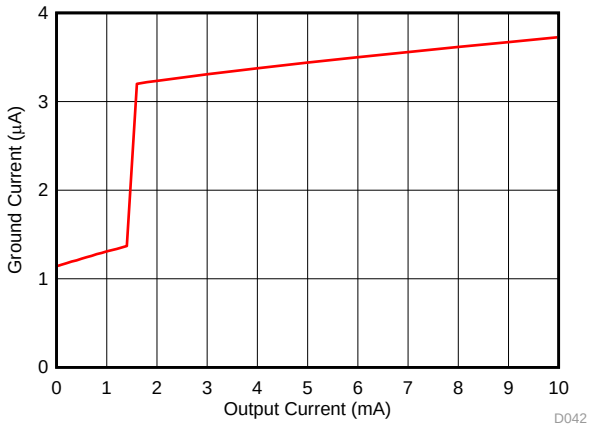


Figure 4. I_{GND} vs I_{OUT} up to 10 mA

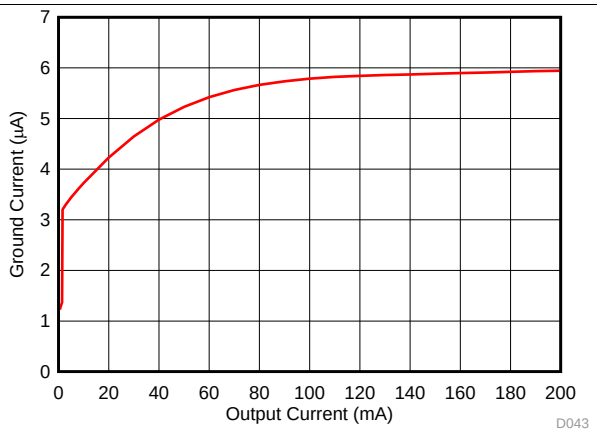


Figure 5. I_{GND} vs I_{OUT} up to 200 mA

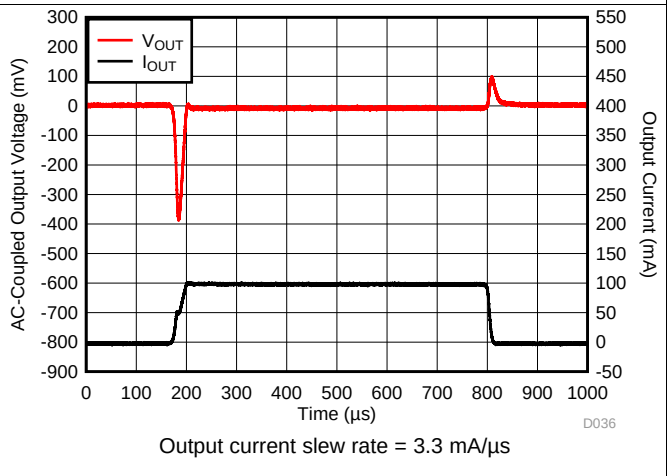
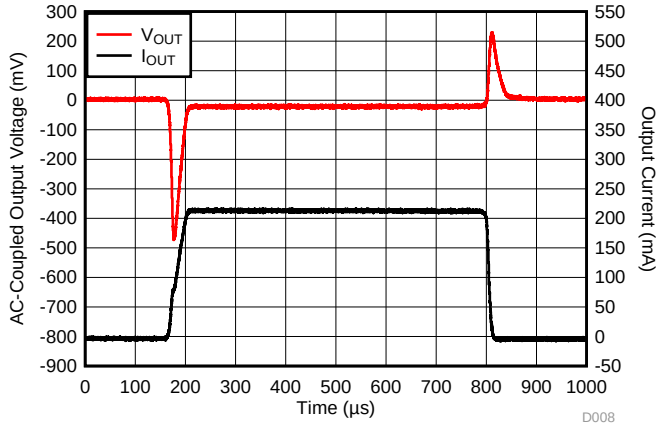


Figure 6. I_{OUT} Transient 0 mA to 100 mA

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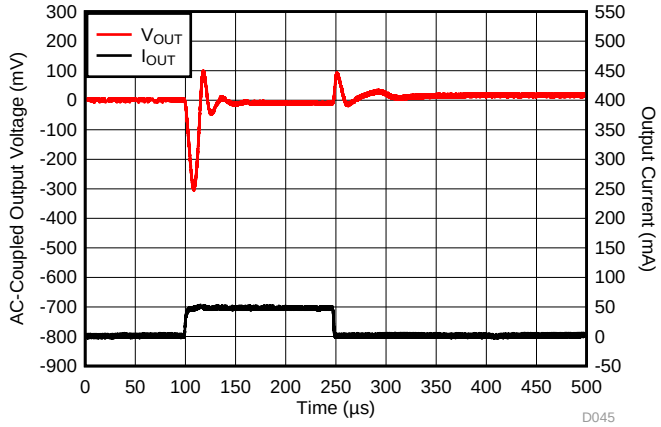
Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)



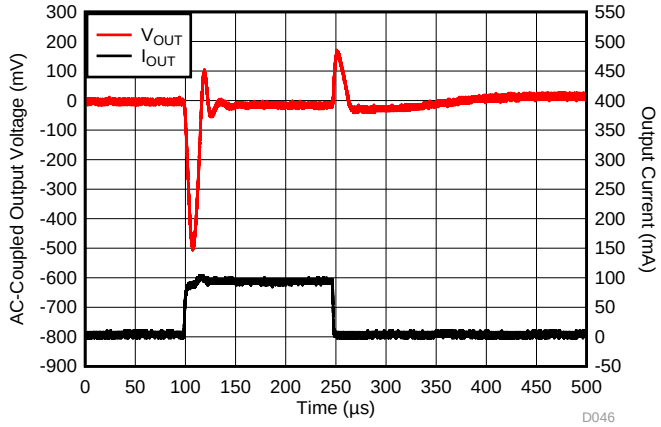
Output current slew rate = 6.6 mA/µs

Figure 7. I_{OUT} Transient 0 mA to 200 mA



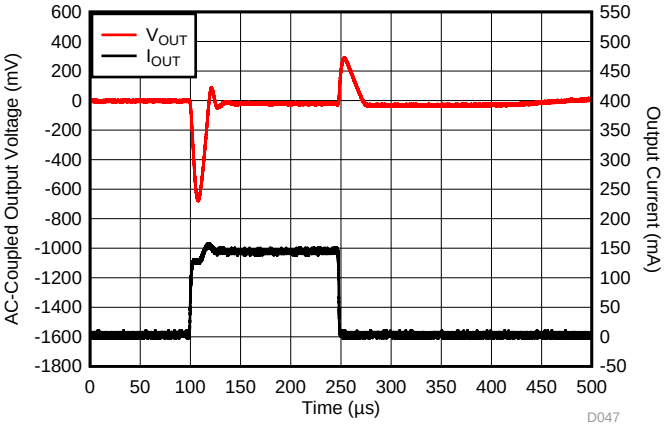
Output current slew rate = 50 mA/µs

Figure 8. I_{OUT} Transient 0 mA to 50 mA



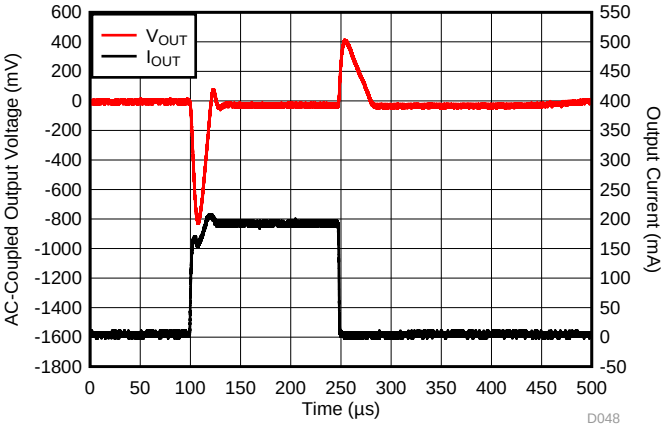
Output current slew rate = 100 mA/µs

Figure 9. I_{OUT} Transient 0 mA to 100 mA



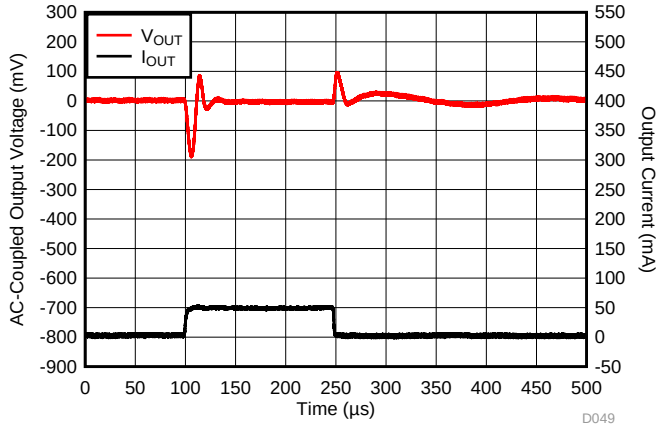
Output current slew rate = 150 mA/µs

Figure 10. I_{OUT} Transient 0 mA to 150 mA



Output current slew rate = 200 mA/µs

Figure 11. I_{OUT} Transient 0 mA to 200 mA



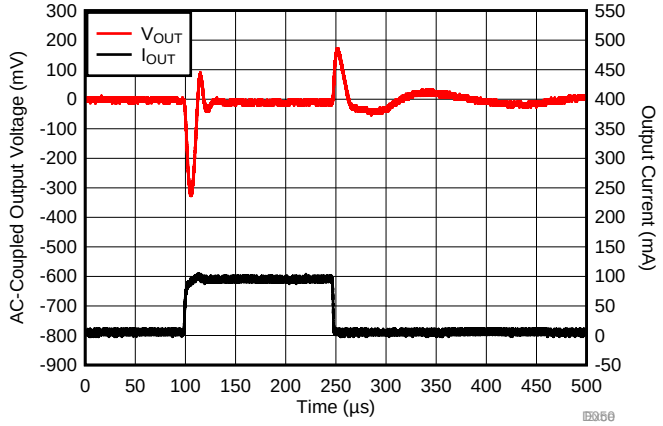
Output current slew rate = 50 mA/µs

Figure 12. I_{OUT} Transient 1 mA to 50 mA

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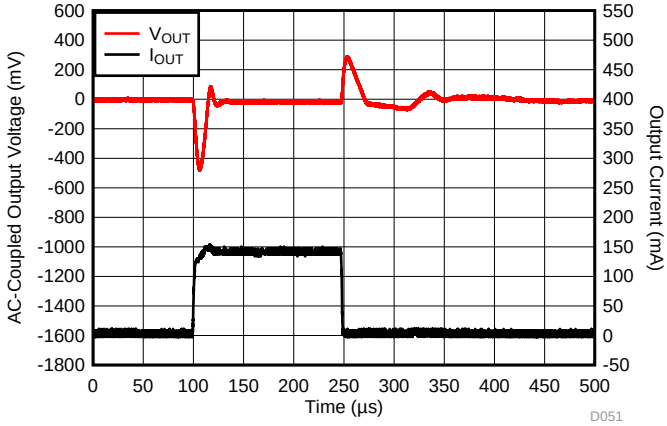
Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)



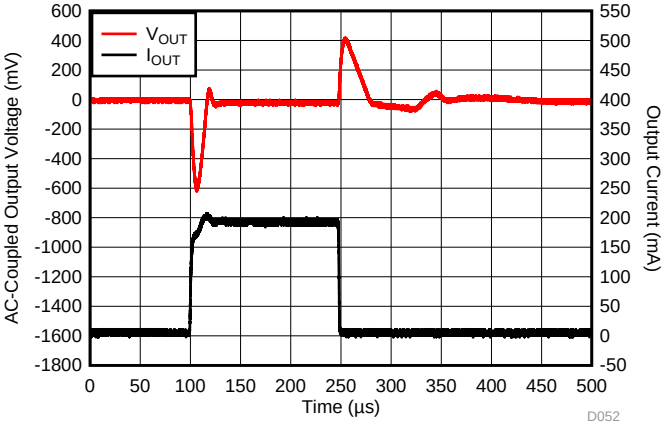
Output current slew rate = 100 mA/µs

Figure 13. I_{OUT} Transient 1 mA to 100 mA



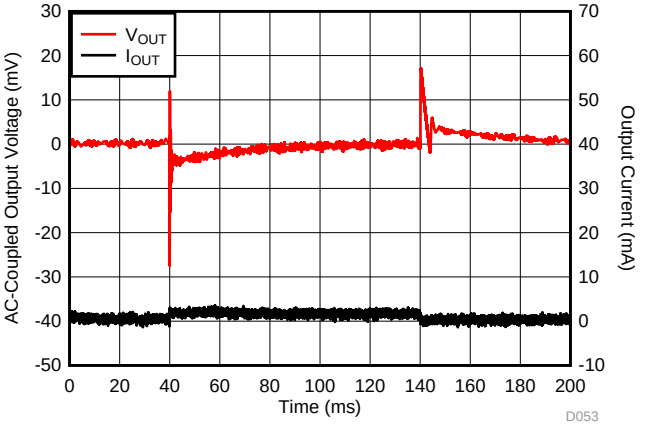
Output current slew rate = 150 mA/µs

Figure 14. I_{OUT} Transient 1 mA to 150 mA



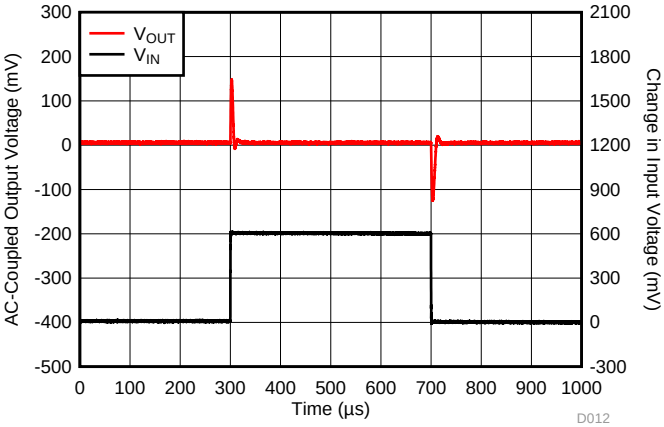
Output current slew rate = 200 mA/µs

Figure 15. I_{OUT} Transient 1 mA to 200 mA



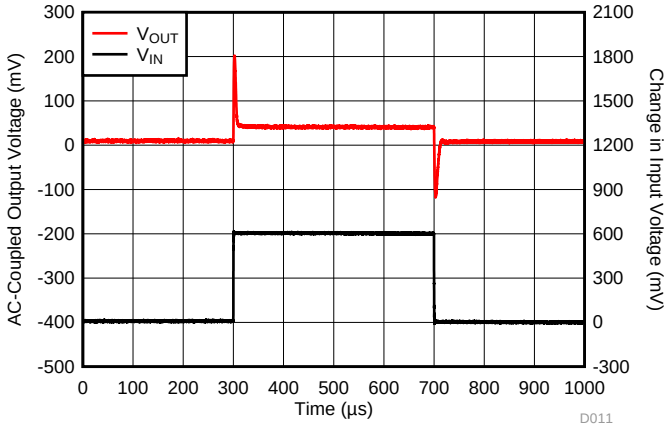
C_{IN} = C_{OUT} = 10 µF, output current slew rate = 3 mA/µs

Figure 16. I_{OUT} Transient 3 µA to 3 mA



I_{OUT} = 100 mA, input voltage slew rate = 0.6 V/µs

Figure 17. V_{IN} Transient



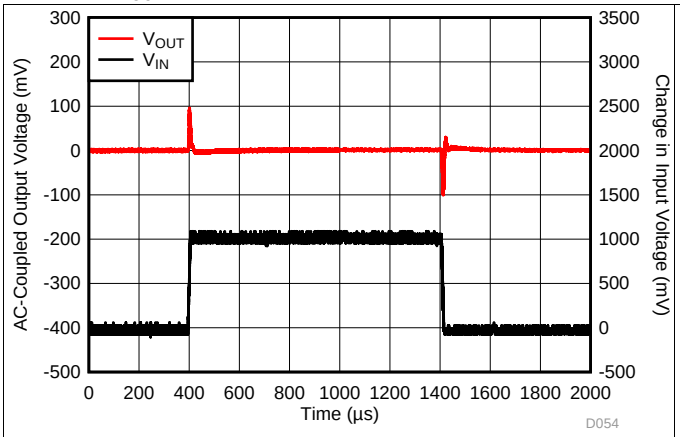
I_{OUT} = 200 mA, input voltage slew rate = 0.6 V/µs

Figure 18. V_{IN} Transient

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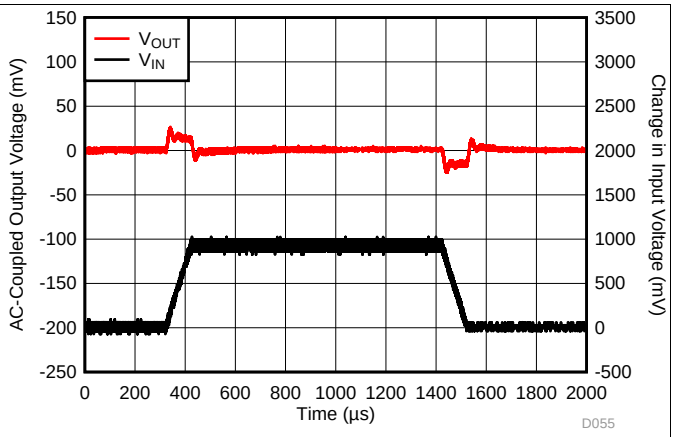
Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)



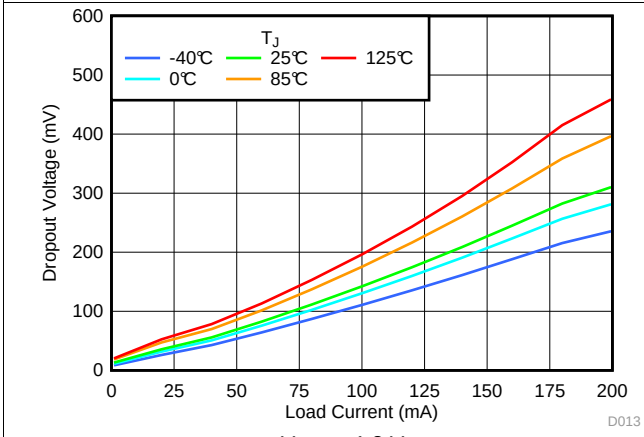
I_{OUT} = 150 mA, input voltage slew rate = 0.1 V/µs

Figure 19. V_{IN} Transient



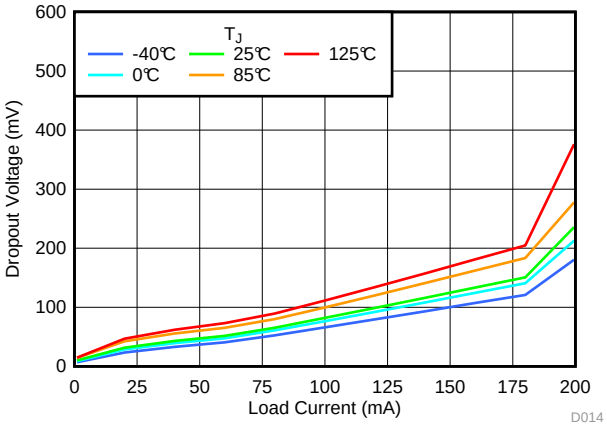
I_{OUT} = 20 mA, input voltage slew rate = 0.01 V/µs

Figure 20. V_{IN} Transient



V_{OUT} = 1.8 V

Figure 21. Dropout vs I_{OUT} and Temperature



V_{OUT} = 3.3 V

Figure 22. Dropout vs I_{OUT} and Temperature

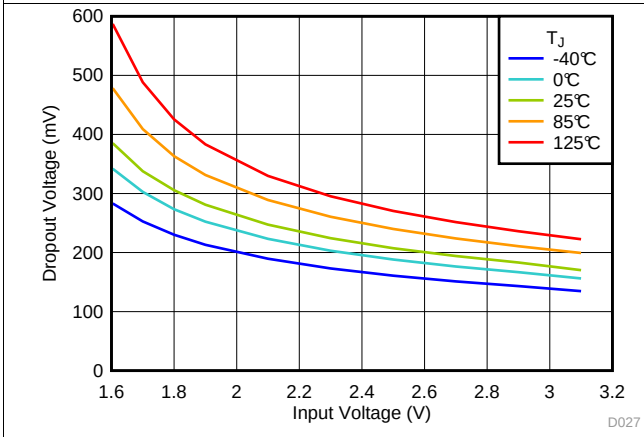
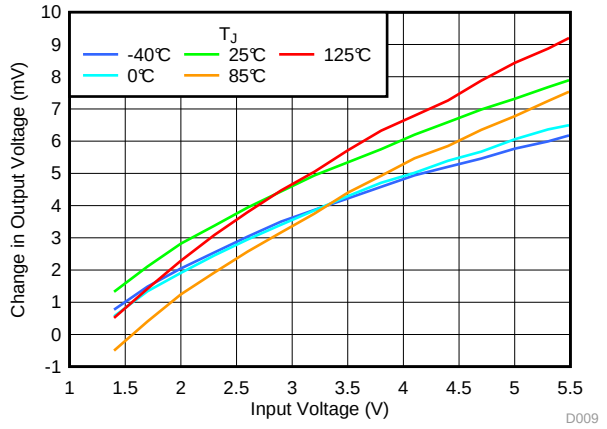


Figure 23. Dropout vs V_{IN} and Temperature

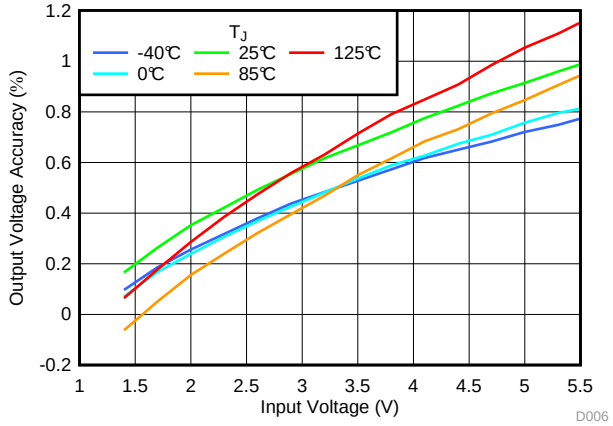


V_{OUT} = 0.8 V

Figure 24. Line Regulation V_{IN} and Temperature

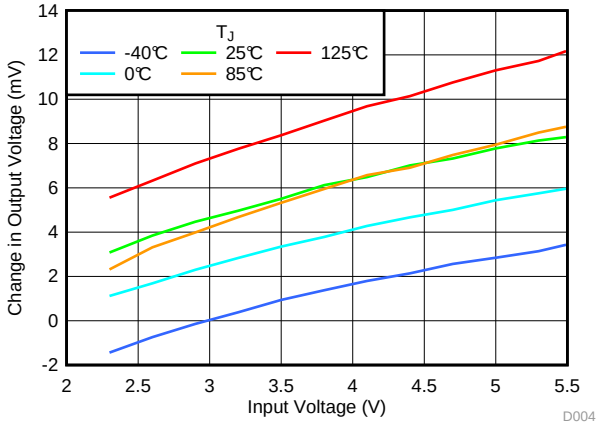
Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)



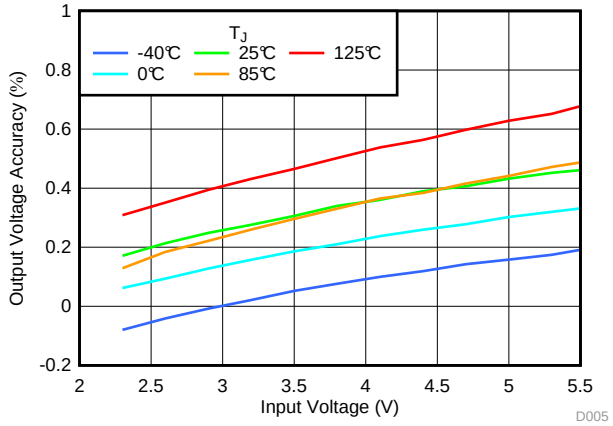
V_{OUT} = 0.8 V

Figure 25. Output Accuracy V_{IN} and Temperature



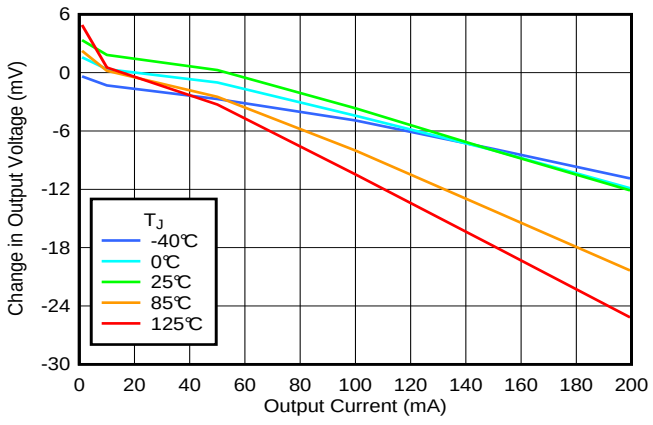
V_{OUT} = 1.8 V

Figure 26. Line Regulation V_{IN} and Temperature



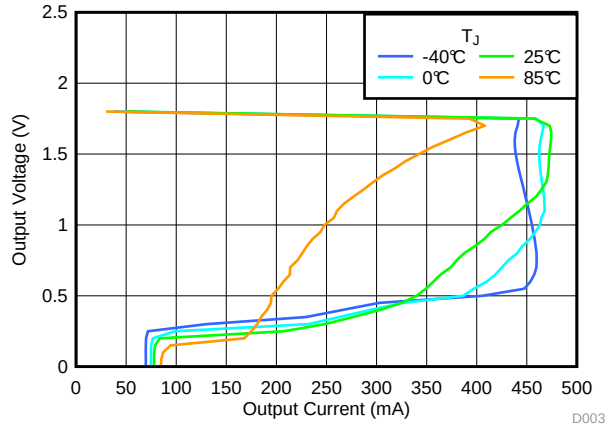
V_{OUT} = 1.8 V

Figure 27. Output Accuracy V_{IN} and Temperature



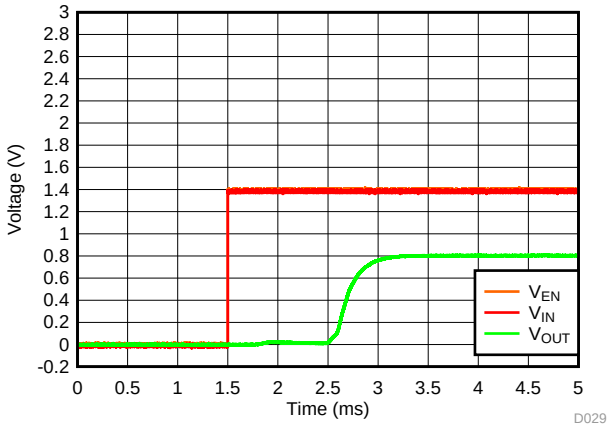
V_{OUT} = 1.8 V

Figure 28. Load Regulation vs I_{OUT} and Temperature



V_{OUT} = 1.8 V

Figure 29. Foldback Current Limit vs I_{OUT} and Temperature



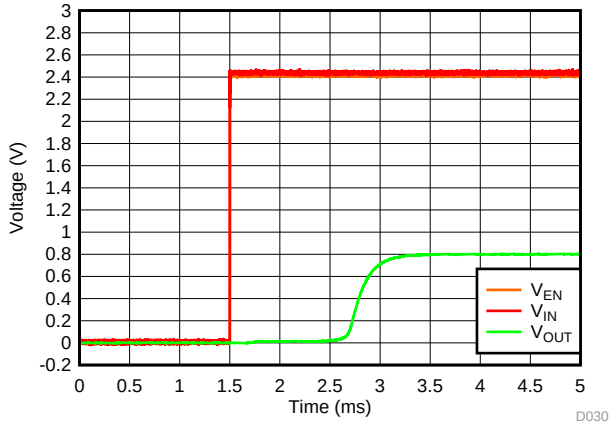
V_{OUT} = 0.8 V, I_{OUT} = 1 mA

Figure 30. Startup With V_{EN} = V_{IN}

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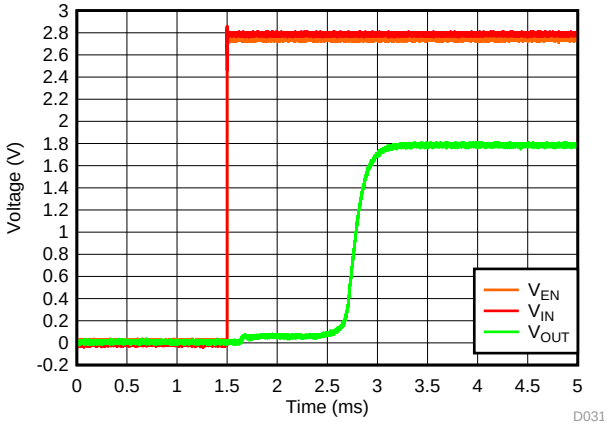
Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)



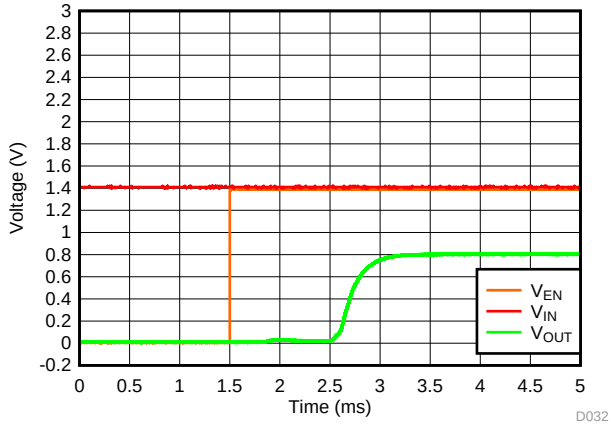
V_{OUT} = 0.8 V, I_{OUT} = 30 mA

Figure 31. Startup With V_{EN} = V_{IN}



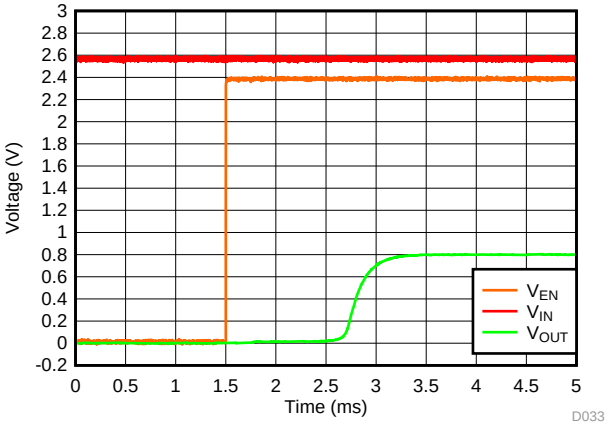
V_{OUT} = 1.8 V, I_{OUT} = 30 mA

Figure 32. Startup With V_{EN} = V_{IN}



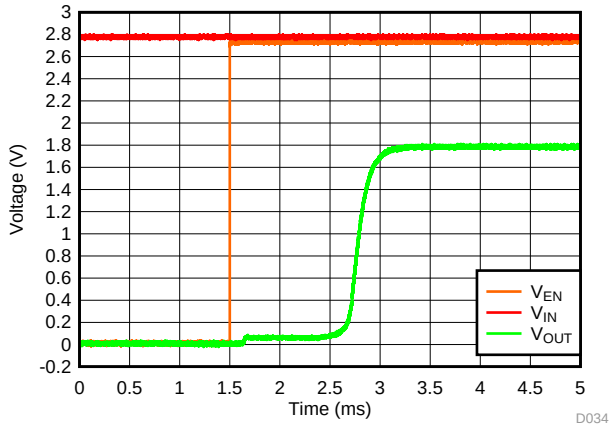
V_{OUT} = 0.8 V, I_{OUT} = 1 mA

Figure 33. Startup With Separate V_{IN} and V_{EN}



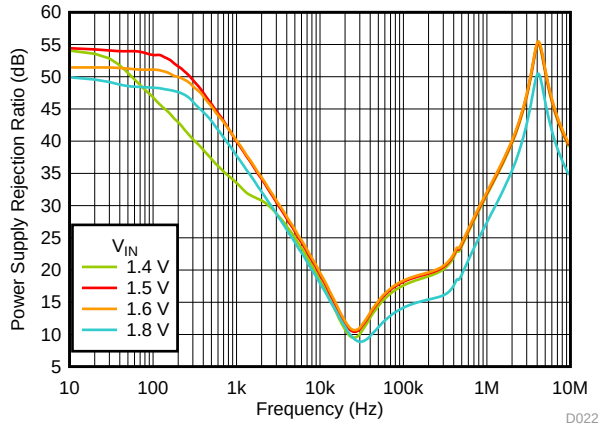
V_{OUT} = 0.8 V, I_{OUT} = 30 mA

Figure 34. Startup With Separate V_{IN} and V_{EN}



V_{OUT} = 1.8 V, I_{OUT} = 30 mA

Figure 35. Startup With Separate V_{IN} and V_{EN}

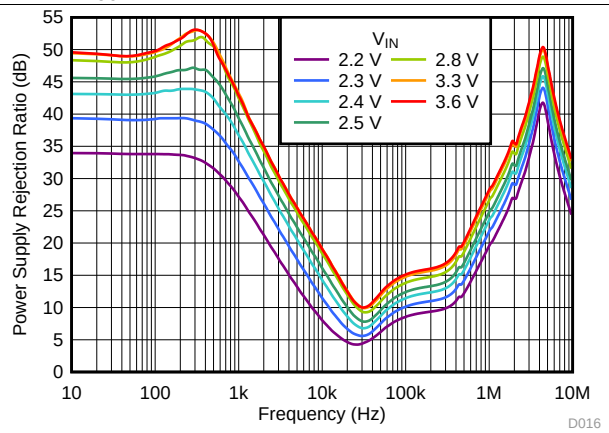


V_{OUT} = 0.8 V, I_{OUT} = 200 mA, C_{OUT} = 1 µF, C_{IN} = 0 µF

Figure 36. PSRR vs Frequency and V_{IN}

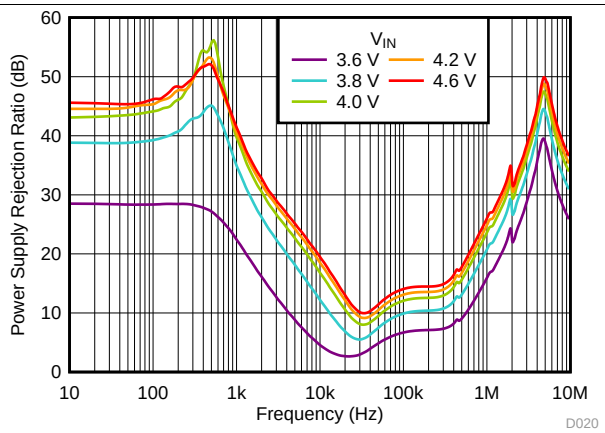
Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)



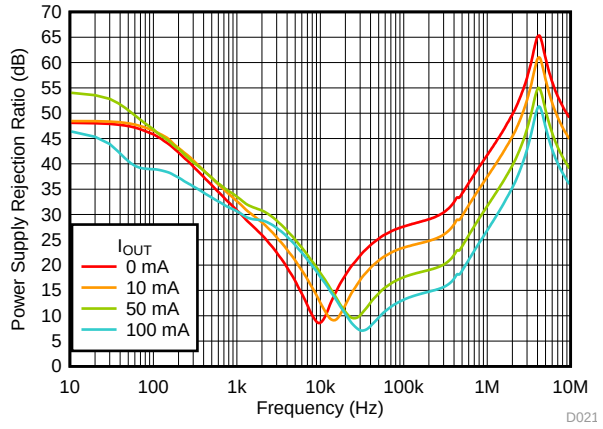
V_{OUT} = 1.8 V, I_{OUT} = 200 mA, C_{OUT} = 1 µF, C_{IN} = 0 µF

Figure 37. PSRR vs Frequency and V_{IN}



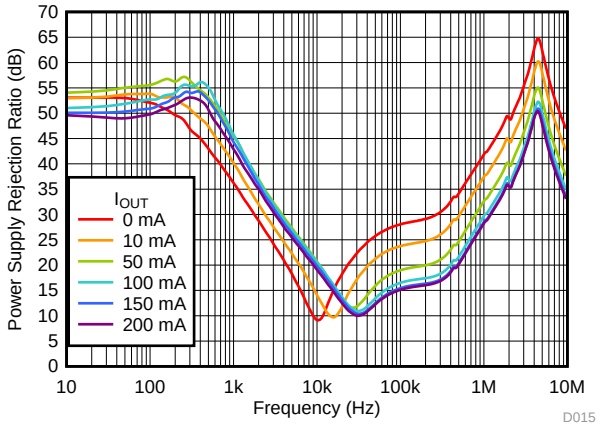
V_{OUT} = 3.3 V, I_{OUT} = 200 mA, C_{OUT} = 1 µF, C_{IN} = 0 µF

Figure 38. PSRR vs Frequency and V_{IN}



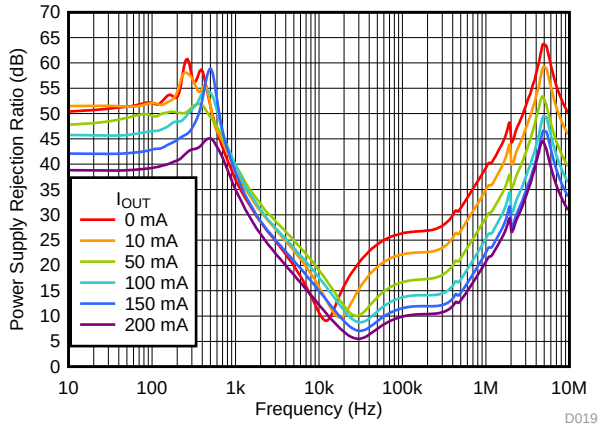
V_{OUT} = 0.8 V, V_{IN} = 1.4 V, C_{OUT} = 1 µF, C_{IN} = 0 µF

Figure 39. PSRR vs Frequency and I_{OUT}



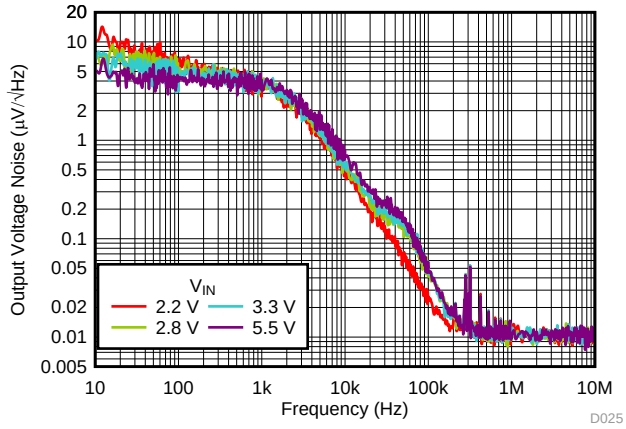
V_{OUT} = 1.8 V, V_{IN} = 2.8 V, C_{OUT} = 1 µF, C_{IN} = 0 µF

Figure 40. PSRR vs Frequency and I_{OUT}



V_{OUT} = 3.3 V, V_{IN} = 3.8 V, C_{OUT} = 1 µF, C_{IN} = 0 µF

Figure 41. PSRR vs Frequency and I_{OUT}



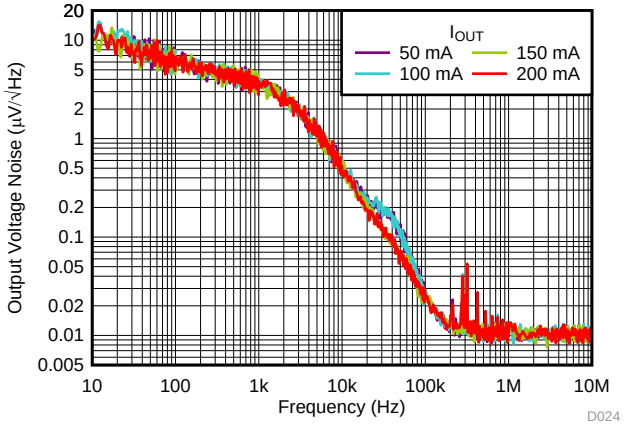
V_{OUT} = 1.8 V, I_{OUT} = 200 mA, C_{OUT} = 1 µF

Figure 42. Output Noise vs Frequency and V_{IN}

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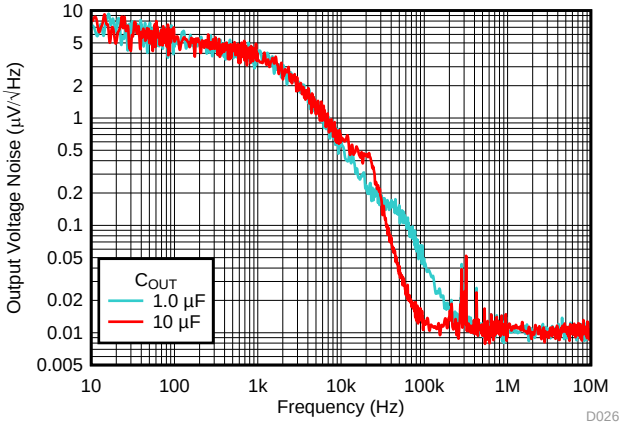
Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)



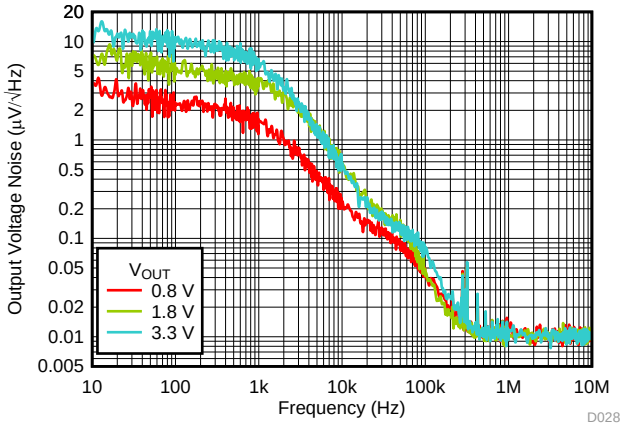
V_{OUT} = 1.8 V, V_{IN} = 2.8 V, C_{OUT} = 1 µF

Figure 43. Output Noise vs Frequency and I_{OUT}



V_{OUT} = 1.8 V, V_{IN} = 2.8 V, I_{OUT} = 200 mA

Figure 44. Output Noise vs Frequency and C_{OUT}



V_{IN} = V_{OUT} + 1 V, I_{OUT} = 200 mA, C_{OUT} = 1 µF

Figure 45. Output Noise vs Frequency and V_{OUT}

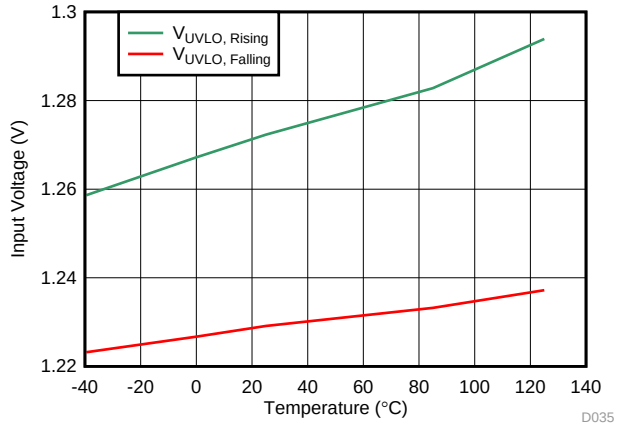


Figure 46. UVLO V_{IN} Rising and Falling Thresholds vs Temperature

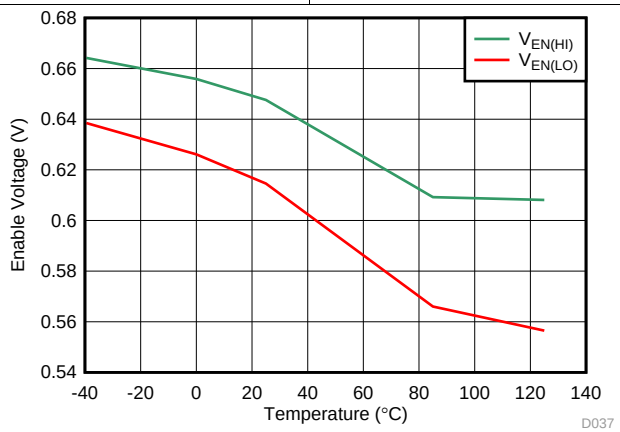


Figure 47. Enable High and Low Thresholds vs Temperature

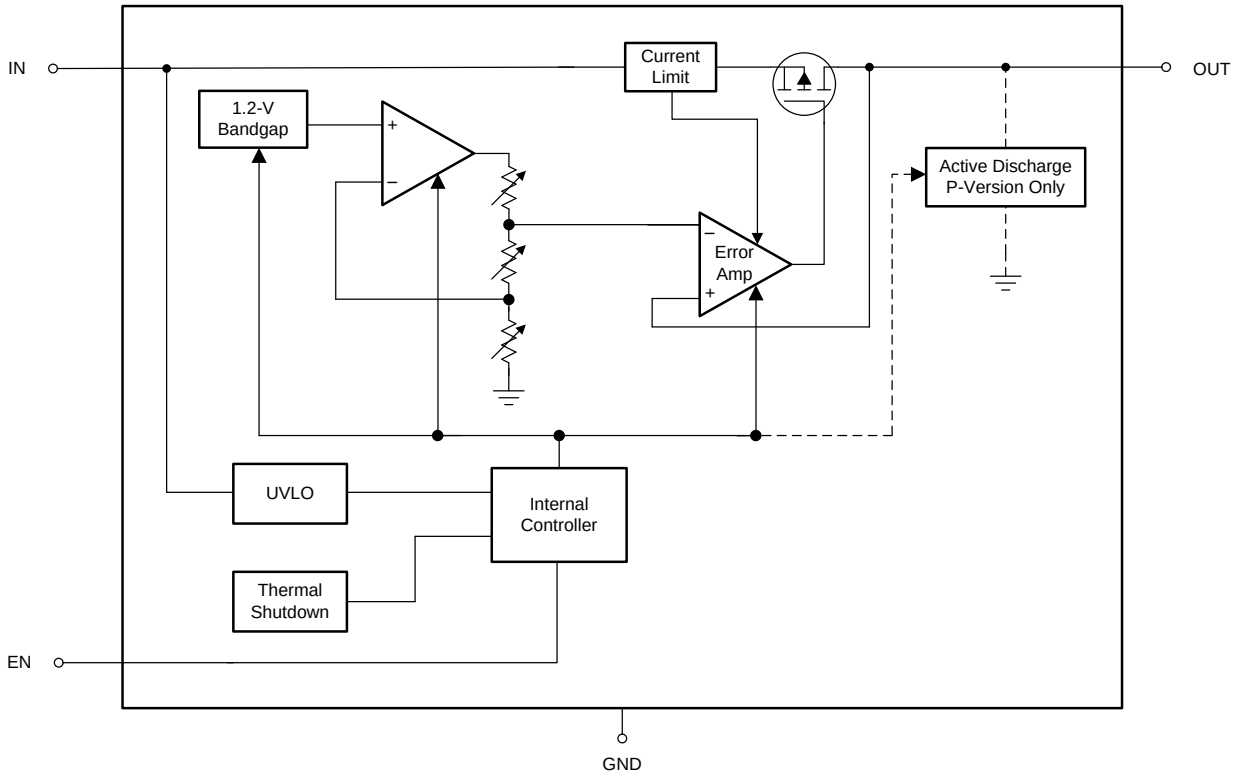
7 Detailed Description

7.1 Overview

The TPS7A05 is a ultra-low I_Q linear voltage regulator that is optimized for excellent transient performance. These characteristics make the TPS7A05 ideal for most battery-powered applications.

This low-dropout regulator (LDO) offers foldback current limit, shutdown, thermal protection, and optional active discharge.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Excellent Transient Response

The device includes several innovative circuits to ensure excellent transient response. Dynamic biasing increases the I_Q for a short duration during transients to extend the closed-loop bandwidth and improve the device response time during transients.

Adaptive biasing increases the I_Q as the dc load current increases, extending the bandwidth of the control loop. The device response time across the output voltage range is constant because of the use of a buffered reference topology, which keeps the control loop in unity gain at any output voltage.

These features give the device a wide loop bandwidth during transients that ensure excellent transient response while maintaining the device low I_Q in steady-state conditions; see the *Application and Implementation* section for more details.

7.3.2 Active Discharge

Devices with this option have an internal pulldown MOSFET that connects a 120-Ω resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated when the device is disabled, in undervoltage lockout (UVLO), or in thermal shutdown.

The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. Equation 1 calculates the time constant:

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device-rated current.

7.3.3 Low I_Q in Dropout

In most LDOs the I_Q significantly increases when the device is placed into dropout, which is especially true for low I_Q LDOs with adaptive biasing. The TPS7A05 detects when operating in dropout and disables the adaptive biasing, minimizing the I_Q increase.

7.3.4 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit monitors the input voltage (V_{IN}) to prevent the device from turning on before V_{IN} rises above the lockout voltage. The UVLO circuit also disables the output of the device when V_{IN} falls below the lockout voltage. If the device includes the optional active discharge, the output is connected to ground with a 120-Ω pulldown resistor when V_{IN} is below the lockout voltage; see the *Application and Implementation* section for more details.

7.3.5 Enable

The enable pin for the device is active high. The output of the device is turned on when the enable pin voltage is greater than the EN pin logic high voltage, and the output of the device is turned off when the enable pin voltage is less than the EN pin logic low voltage. A voltage less than the EN pin logic low voltage on the enable pin disables all internal circuits.

At the next turn-on, any voltage on the EN pin below the logic low voltage ensures a normal start-up waveform with start-up ramp rate control, provided there is enough time to discharge the output capacitance. If shutdown capability is not required, connect EN to IN. V_{EN} must not exceed V_{IN}.

7.3.6 Internal Foldback Current Limit

The internal foldback current-limit circuit is used to protect the LDO against high-load current faults or shorting events. The foldback mechanism lowers the current limit as the output voltage decreases, and limits power dissipation during short-circuit events while still allowing for the device to operate at its rated output current; see Figure 29.

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Feature Description (continued)

A foldback example for this device is that when V_{OUT} is 90% of $V_{OUT(nom)}$ the current limit is I_{CL}(typical); however, if V_{OUT} is forced to 0 V the current limit is I_{SC} (typical).

In many LDOs the foldback current limit can prevent start-up into a constant-current load or a negatively-biased output. The foldback mechanism for this device goes into a brick-wall current limit when V_{OUT} > 500 mV (typ), thus limiting current to I_{CL}(typical) and, when V_{OUT} is approximately 0 V, current is limited to I_{SC} (typical) to ensure normal start-up into a variety of loads.

The foldback current limit is disengaged when I_{OUT} < 1 mA (typical) to reduce I_Q. As such, the current-limit loop takes longer to respond to a current-limit event when I_{OUT} < 1 mA (typ).

Thermal shutdown can activate during a current-limit event because of the high power dissipation typically found in these conditions. To ensure proper operation of the current limit, minimize the inductances to the input and load. Continuous operation in current limit is not recommended.

7.3.7 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when thermal junction temperature (T_J) of the main pass-FET rises to $T_{sd(Shutdown)}$ (typical). Thermal shutdown hysteresis assures that the LDO resets again (turns on) when the temperature falls to $T_{sd(Reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, and thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced.

For reliable operation, limit the junction temperature to a maximum of 125°C. Operation above 125°C causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above a junction temperature of 125°C reduces long-term reliability.

A fast start-up when T_J > $T_{sd(Reset)}$ (typical, outside of the specified operating range) causes the device thermal shutdown to assert at $T_{sd(Reset)}$ and prevents the device from turning on until the junction temperature is reduced below $T_{sd(Shutdown)}$.

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7.4 Device Functional Modes

The device has several modes of operation,:

- Normal operation: The device regulates to the nominal output voltage
- Dropout operation: The pass element operates as a resistor and the output voltage is set as $V_{IN} – V_{DO}$
- Shutdown: The output of the device is disabled and the discharge circuit is activated

Table 1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{sd(Shutdown)}$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{sd(Shutdown)}$
Disabled mode (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LO)}$	—	$T_J > T_{sd(Shutdown)}$

7.4.1 Normal Mode

The device regulates the output to the nominal output voltage when all normal mode conditions in Table 1 are met.

7.4.2 Dropout Mode

The device is not in regulation, and the output voltage tracks the input voltage minus the voltage drop across the pass transistor of the device. In this mode, the PSRR, noise, and transient performance of the device are significantly degraded.

7.4.3 Disable Mode

In this mode, the pass element is turned off, the internal circuits are shut down, and the output voltage is actively discharged to ground by an internal resistor.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, assume effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

8.1.3 Special Considerations When Ramping Down V_{IN} and Enable

Care must be taken when ramping down voltage on the IN and EN pins to power-down the device when the operating free-air temperature is less than 15°C. The minimum ramp-down time for the IN pin is 10 ms. The minimum ramp-down time for the EN pin is 100 µs. Ramping at faster rates can cause the regulator to exhibit undesired startup behavior on the next power-on.

If V_{IN} is ramped down faster than 10 ms, the next startup may exhibit a partial startup, shutoff, followed by a normal soft-start startup. Figure 48 shows this response.

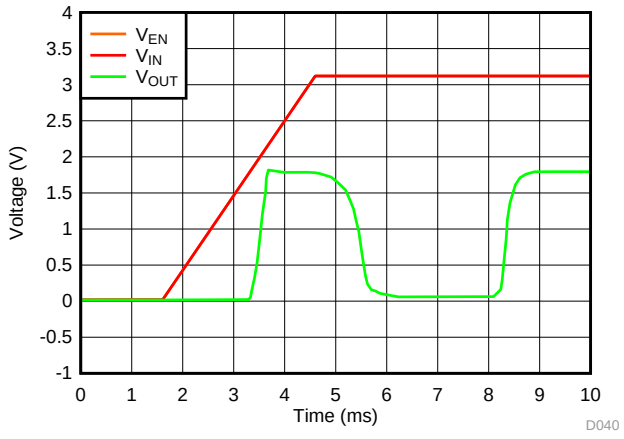


Figure 48. Partial Startup, Shutdown, Normal Startup With V_{EN} = V_{IN}

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Application Information (continued)

If the EN pin is ramped down faster than 100 µs, the next startup may exhibit a delay time of up to 130 ms before the output ramps up with a normal soft-start startup. Figure 49 shows this delay.

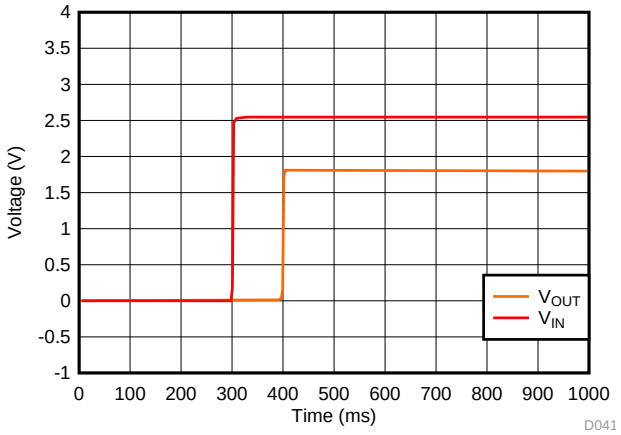


Figure 49. Long Delay to Startup With $V_{EN} = V_{IN}$

Fast ramp downs of V_{IN} and the EN pin charge internal high-impedance nodes in the device, which take extended time to discharge below 15°C. To avoid these startup behaviors, follow the recommended minimum ramp down times for V_{IN} and the EN pin.

8.1.4 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. See Figure 6 for typical load transient response. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions in Figure 50 are broken down as described in this section. Regions A, E, and H are where the output voltage is in steady-state.

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

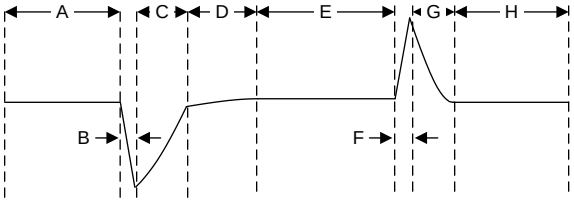


Figure 50. Load Transient Waveform

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Application Information (continued)

8.1.5 Dropout Voltage

The device uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass transistor is in the linear region of operation, and the input-to-output resistance of the device is the drain-to-source resistance of the PMOS pass transistor. V_{DO} scales with the output current and changes with temperature because the PMOS pass transistor functions like a resistor in dropout mode. For a graph of dropout voltage, see Figure 22. As with any linear regulator, PSRR and the transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation. See Figure 23 for dropout performance.

8.1.5.1 Behavior When Transitioning From Dropout Into Regulation

Some applications may have transients that place the device into dropout, especially as this device can be powered from a battery with high ESR. A typical application with these conditions is using a stack of two 1.55-V coin-cell batteries with an ESR of 30 Ω to create a 2.5-V rail and experiencing a load transient from 1 µA to 25 mA. This load transient causes the input supply to drop 750 mV, placing the device into dropout.

The load transient saturates the output stage of the error amplifier when the pass element is driven fully on, making the pass element function like a resistor from V_{IN} to V_{OUT}. The error amplifier response time to this load transient is limited because the error amplifier must first recover from saturation and then place the pass element back into active mode. During this time V_{OUT} overshoots because the pass element is functioning as a resistor from V_{IN} to V_{OUT}. This device uses a loop pulldown circuit to help mitigate the overshoot.

If operating under these conditions, applying a higher dc load or increasing the output capacitance reduces the overshoot because these solutions provide a path to dissipate the excess charge.

8.1.5.2 Behavior of Output Resulting From Line Transient When in Dropout

The output deviation resulting from a line transient can be significantly higher when the device is operating in dropout. As explained in the *Dropout Voltage* section, the response time of the error amplifier is limited when in dropout, so the output deviation is larger and can exceed twice the regulated output voltage. Care must be taken in applications where line transients are expected when the device is operating in dropout.

8.1.6 Undervoltage Lockout (UVLO) Operation

The UVLO circuit ensures that the device stays disabled before its input supply reaches the minimum operational voltage range, and ensures that the device shuts down when the input supply collapses. See Figure 46 for rising and falling thresholds. Figure 51 depicts the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold
- Region B: Normal operation, regulating device
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hystersis). The output may fall out of regulation but the device is still enabled.
- Region D: Normal operation, regulating device
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls as a result of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold
- Region G: The device is disabled as the input voltage falls below the UVLO falling threshold to 0 V. The output falls as a result of the load and active discharge circuit.

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Application Information (continued)

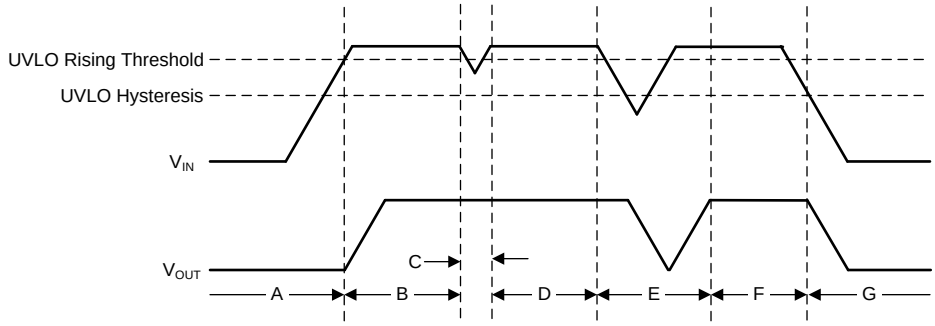


Figure 51. Typical UVLO Operation

8.1.7 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

Equation 2 calculates the maximum allowable power dissipation for the device in a given package:

$$P_{D\text{-}MAX} = ((T_J - T_A) / R_{\theta JA}) \quad (2)$$

Equation 3 represents the actual power being dissipated in the device:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (3)$$

An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A05 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device depends on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to Equation 4, maximum power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A). The equation is rearranged in Equation 5 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (4)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (5)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the DQN package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

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Application Information (continued)

8.1.7.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with Equation 6 and are given in the *Thermal Information* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \quad (6)$$

where:

- P_D is the power dissipated as explained in Equation 3
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

8.1.7.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is shown in Figure 52 and can be separated into the following regions:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} – V_{OUT}$) at a given output current level; see the *Dropout Voltage* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - Equation 5 provides the shape of the slope. The slope is nonlinear because the maximum rated junction temperature of the LDO is controlled by the power dissipation across the LDO, thus when $V_{IN} – V_{OUT}$ increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} – V_{OUT}$.

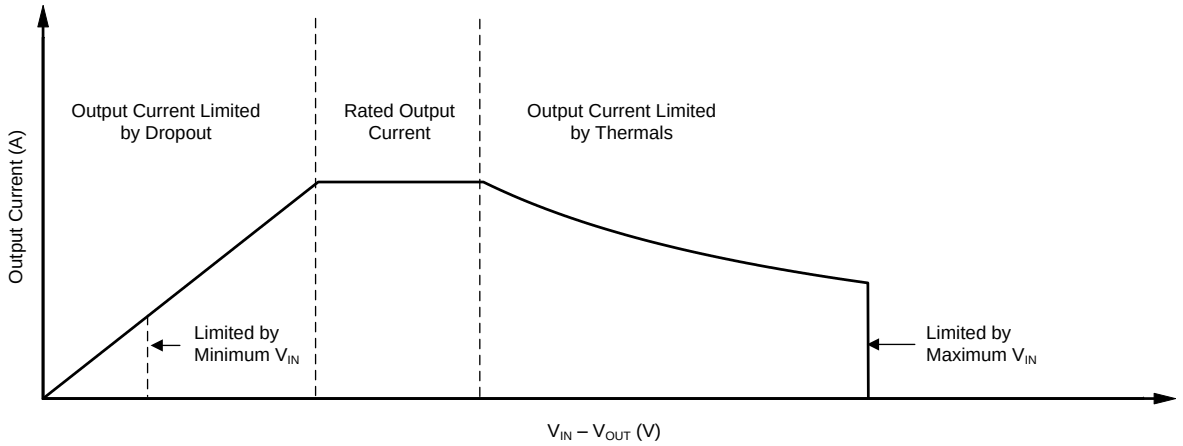


Figure 52. Region Description for Continuous Operation

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8.2 Typical Application

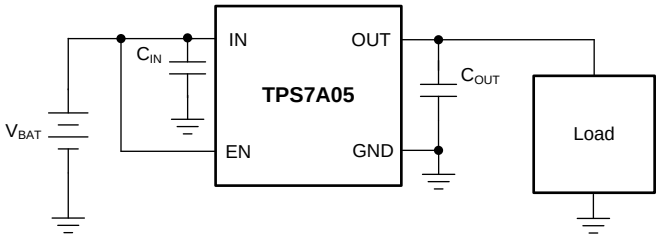


Figure 53. Operation From the Battery Input Supply

8.2.1 Design Requirements

Table 2 summarizes the design requirements for Figure 53.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.0 V to 2.0 V (CR2032 battery)
Output voltage	1.0 V, ±2% (T_J from –40 to +85ºC)
Output load	10 mA

8.2.2 Design Considerations

For this design example, the 1.0-V, fixed-version TPS7A0510 device is selected. A single CR2032 coin-cell battery was used, thus a 1.0-µF input capacitor is recommended to minimize transient currents drawn from the battery. A 1.0-µF output capacitor is also recommended for excellent load transient response. The dropout voltage (V_{DO}) is kept within the TPS7A05 dropout voltage specification for the 1.0-V output voltage option to keep the device in regulation under all load and temperature conditions for this design. The very small ground current consumed by the regulator shown in Figure 54 allows for long battery life.

8.2.3 Application Curve

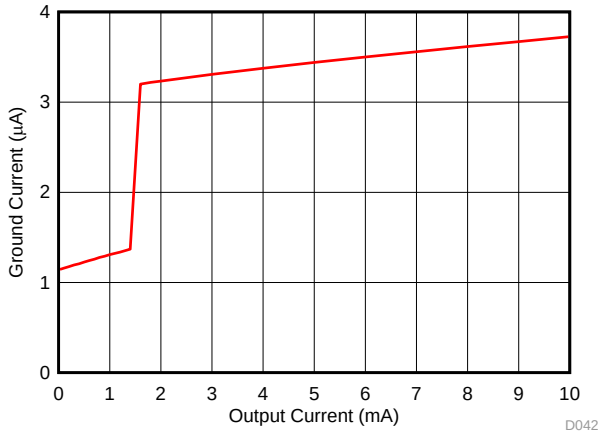


Figure 54. I_{GND} vs I_{OUT} at 25°C

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.4 V to 5.5 V. The input supply must be well regulated and free of spurious noise. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 0.5 V. A 1 µF or greater input capacitor is recommended to be used to reduce the impedance of the input supply, especially during transients.

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10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible
- Use copper planes for device connections to optimize thermal performance
- Place thermal vias around the device to distribute heat
- Do not place a thermal via directly beneath the thermal pad of the DQN package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

10.2 Layout Example

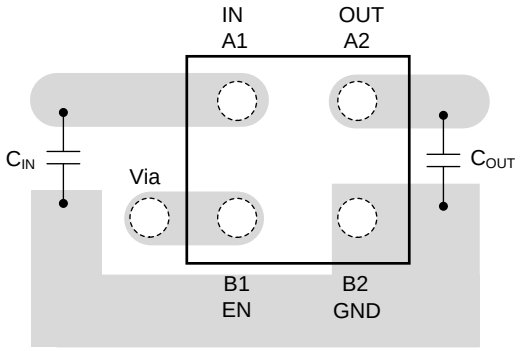


Figure 55. Layout Example for the YKA Package

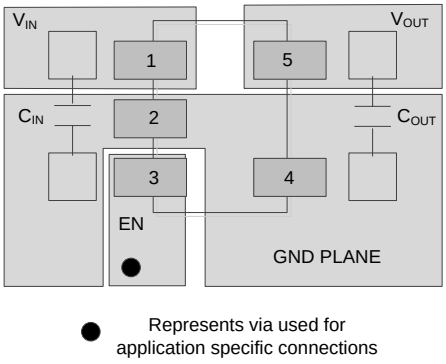


Figure 56. Layout Example for the DBV Package

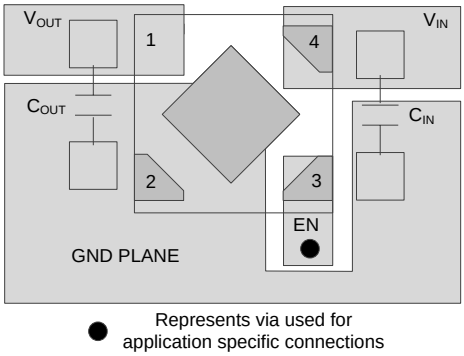


Figure 57. Layout Example for the DQN Package

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Spice Models

SPICE models for the TPS7A05 are available through the product folder under *Tools & software*.

11.1.2 Device Nomenclature

Table 3. Device Nomenclature(1)(2)

PRODUCT	V_{OUT}
TPS7A05**xx(x)Pyyyz**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **P** is optional; P indicates an active output discharge feature. **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.0 V to 3.3 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Universal Low-Dropout (LDO) Linear Voltage Regulator MultiPkgLDOEVM-823 Evaluation Module

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PS7A0508PDBZR	ACTIVE	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PS7A0512PDBZR	ACTIVE	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PS7A0518PDBZR	ACTIVE	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PS7A0528PDBZR	ACTIVE	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PS7A0530PDBZR	ACTIVE	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PS7A0533PDBZR	ACTIVE	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TPS7A0508PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1C6F	Samples
TPS7A0508PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1C6F	Samples
TPS7A0508PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	6G	Samples
TPS7A0508PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	6G	Samples
TPS7A0508PYKAR	ACTIVE	DSBGA	YKA	4	12000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	3	Samples
TPS7A0510PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IKF	Samples
TPS7A0510PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IKF	Samples
TPS7A0510PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C7	Samples
TPS7A0510PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C7	Samples
TPS7A0510PYKAR	ACTIVE	DSBGA	YKA	4	12000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	L	Samples
TPS7A0512PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ILF	Samples
TPS7A0512PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ILF	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A0512PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C8	Samples
TPS7A0512PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C8	Samples
TPS7A0512PYKAR	ACTIVE	DSBGA	YKA	4	12000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	M	Samples
TPS7A0515PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IMF	Samples
TPS7A0515PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IMF	Samples
TPS7A0515PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C9	Samples
TPS7A0515PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C9	Samples
TPS7A0515PYKAR	ACTIVE	DSBGA	YKA	4	12000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	N	Samples
TPS7A051825PYKAR	ACTIVE	DSBGA	YKA	4	12000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	P	Samples
TPS7A0518PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1INF	Samples
TPS7A0518PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1INF	Samples
TPS7A0518PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CA	Samples
TPS7A0518PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CA	Samples
TPS7A0518PYKAR	ACTIVE	DSBGA	YKA	4	12000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	P	Samples
TPS7A0522PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1P3F	Samples
TPS7A0522PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1P3F	Samples
TPS7A0525PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IOF	Samples
TPS7A0525PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IOF	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A0525PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CB	Samples
TPS7A0525PDQNR3	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CB	
TPS7A0525PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CB	Samples
TPS7A0525PYKAR	ACTIVE	DSBGA	YKA	4	12000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Q	Samples
TPS7A05285PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IRF	Samples
TPS7A05285PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IRF	Samples
TPS7A05285PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC	Samples
TPS7A05285PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC	Samples
TPS7A05285PYKAR	ACTIVE	DSBGA	YKA	4	12000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	R	Samples
TPS7A0528PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DH	Samples
TPS7A0528PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DH	Samples
TPS7A0530PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1QWF	Samples
TPS7A0530PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1QWF	Samples
TPS7A0530PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DG	Samples
TPS7A0530PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DG	Samples
TPS7A0530PYKAR	ACTIVE	DSBGA	YKA	4	12000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	W	Samples
TPS7A0531PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1P4F	Samples
TPS7A0531PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1P4F	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A0533PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IPF	Samples
TPS7A0533PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IPF	Samples
TPS7A0533PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD	Samples
TPS7A0533PDQNR3	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD	
TPS7A0533PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD	Samples
TPS7A0533PYKAR	ACTIVE	DSBGA	YKA	4	12000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

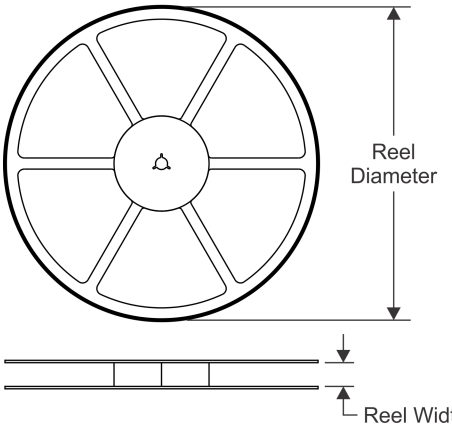
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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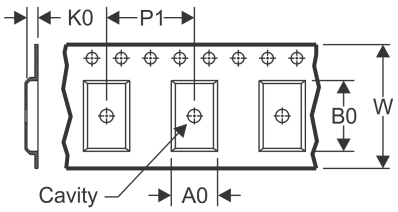
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

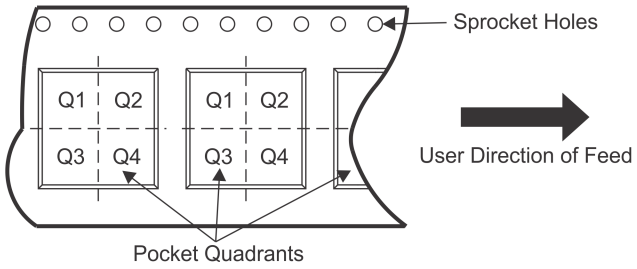


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

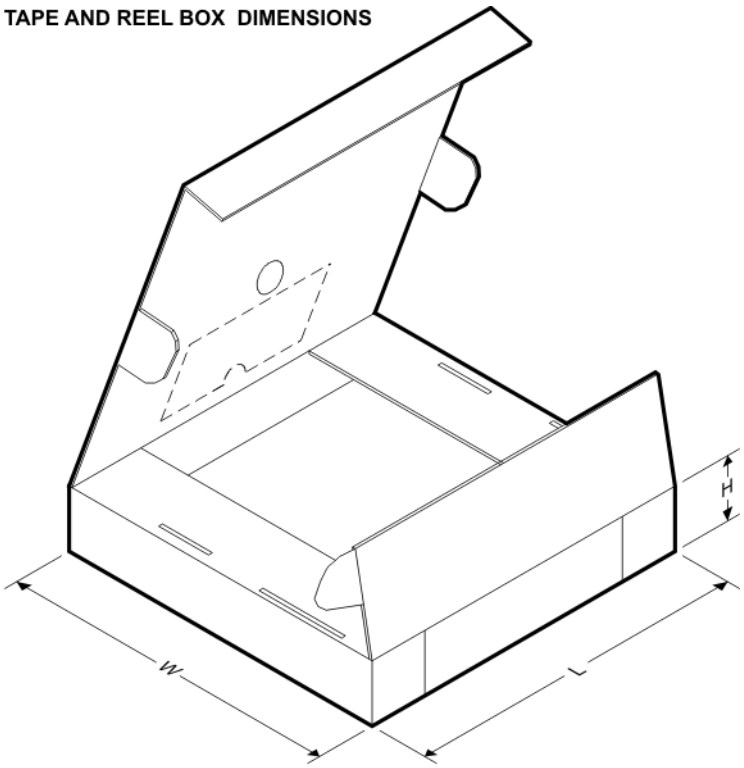


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A0508PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0508PDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0508PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0508PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0508PYKAR	DSBGA	YKA	4	12000	180.0	8.4	0.76	0.76	0.46	2.0	8.0	Q1
TPS7A0510PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0510PDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0510PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0510PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0510PYKAR	DSBGA	YKA	4	12000	180.0	8.4	0.76	0.76	0.46	2.0	8.0	Q1
TPS7A0512PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0512PDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0512PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0512PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0512PYKAR	DSBGA	YKA	4	12000	180.0	8.4	0.76	0.76	0.46	2.0	8.0	Q1
TPS7A0515PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0515PDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0515PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A0515PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0515PYKAR	DSBGA	YKA	4	12000	180.0	8.4	0.76	0.76	0.46	2.0	8.0	Q1
TPS7A051825PYKAR	DSBGA	YKA	4	12000	180.0	8.4	0.76	0.76	0.46	2.0	8.0	Q1
TPS7A0518PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0518PDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0518PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0518PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0518PYKAR	DSBGA	YKA	4	12000	180.0	8.4	0.76	0.76	0.46	2.0	8.0	Q1
TPS7A0522PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0522PDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0525PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0525PDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0525PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0525PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0525PYKAR	DSBGA	YKA	4	12000	180.0	8.4	0.76	0.76	0.46	2.0	8.0	Q1
TPS7A05285PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A05285PDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A05285PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A05285PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A05285PYKAR	DSBGA	YKA	4	12000	180.0	8.4	0.76	0.76	0.46	2.0	8.0	Q1
TPS7A0528PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0528PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0530PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0530PDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0530PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0530PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0530PYKAR	DSBGA	YKA	4	12000	180.0	8.4	0.76	0.76	0.46	2.0	8.0	Q1
TPS7A0531PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0531PDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0533PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0533PDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0533PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0533PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0533PYKAR	DSBGA	YKA	4	12000	180.0	8.4	0.76	0.76	0.46	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A0508PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A0508PDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS7A0508PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0508PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TPS7A0508PYKAR	DSBGA	YKA	4	12000	182.0	182.0	20.0
TPS7A0510PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A0510PDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS7A0510PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0510PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TPS7A0510PYKAR	DSBGA	YKA	4	12000	182.0	182.0	20.0
TPS7A0512PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A0512PDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS7A0512PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0512PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TPS7A0512PYKAR	DSBGA	YKA	4	12000	182.0	182.0	20.0
TPS7A0515PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A0515PDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS7A0515PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0515PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TPS7A0515PYKAR	DSBGA	YKA	4	12000	182.0	182.0	20.0

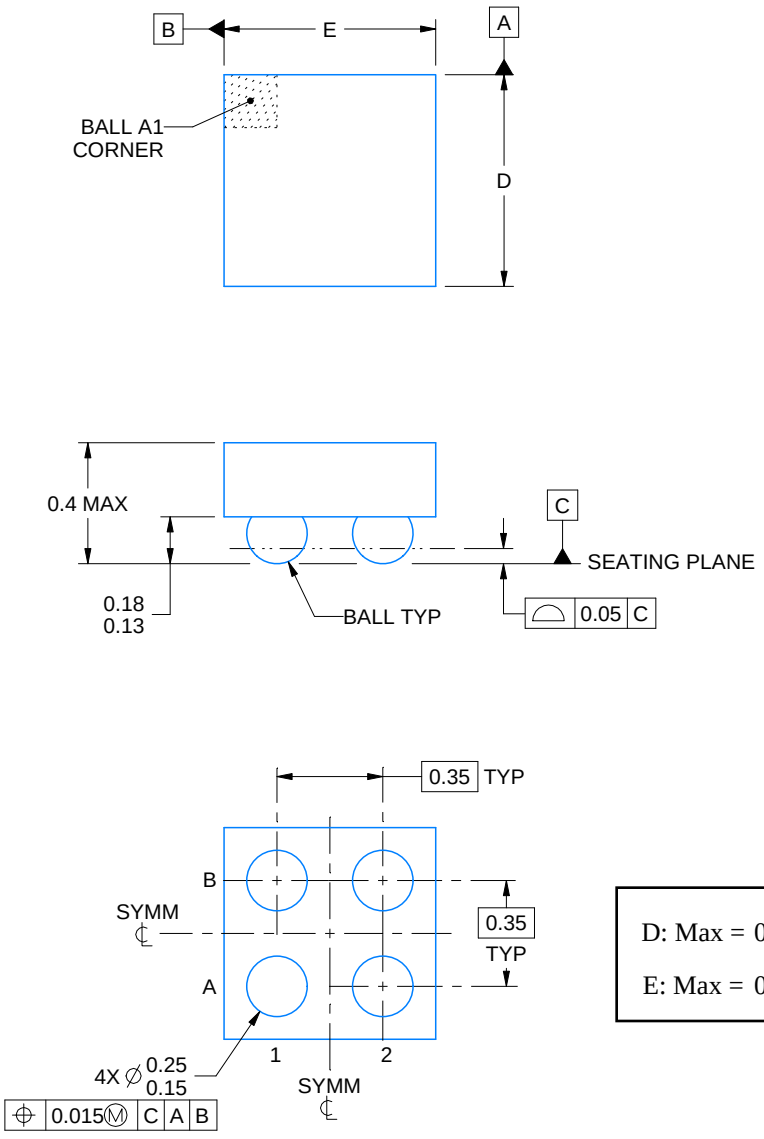
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A051825PYKAR	DSBGA	YKA	4	12000	182.0	182.0	20.0
TPS7A0518PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A0518PDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS7A0518PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0518PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TPS7A0518PYKAR	DSBGA	YKA	4	12000	182.0	182.0	20.0
TPS7A0522PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A0522PDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS7A0525PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A0525PDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS7A0525PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0525PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TPS7A0525PYKAR	DSBGA	YKA	4	12000	182.0	182.0	20.0
TPS7A05285PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A05285PDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS7A05285PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A05285PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TPS7A05285PYKAR	DSBGA	YKA	4	12000	182.0	182.0	20.0
TPS7A0528PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0528PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TPS7A0530PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A0530PDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS7A0530PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0530PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TPS7A0530PYKAR	DSBGA	YKA	4	12000	182.0	182.0	20.0
TPS7A0531PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A0531PDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS7A0533PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A0533PDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS7A0533PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0533PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TPS7A0533PYKAR	DSBGA	YKA	4	12000	182.0	182.0	20.0

PACKAGE OUTLINE

YKA0004

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



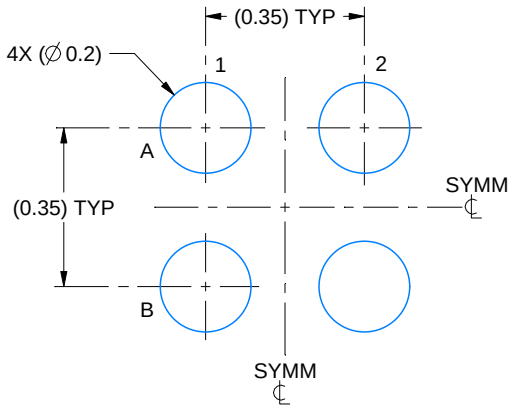
D: Max = 0.694 mm, Min =0.634 mm

E: Max = 0.694 mm, Min =0.634 mm

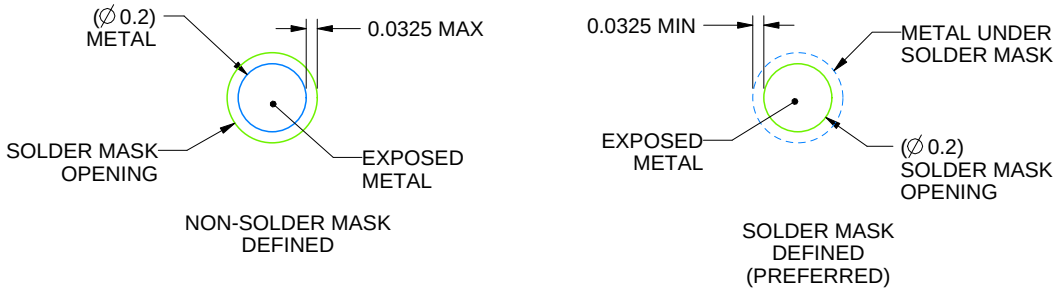
4221909/B 08/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

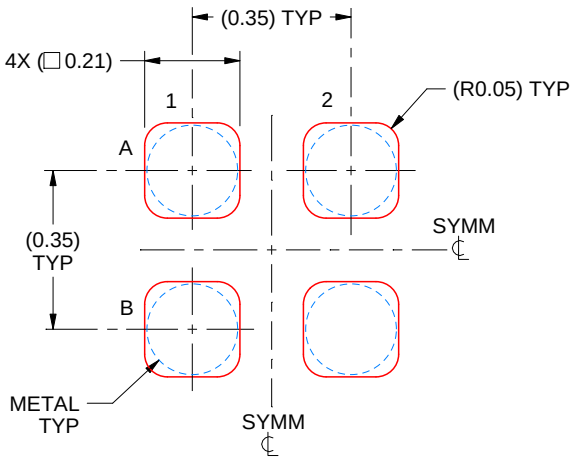


SOLDER MASK DETAILS
NOT TO SCALE

4221909/B 08/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:60X

4221909/B 08/2018

NOTES: (continued)

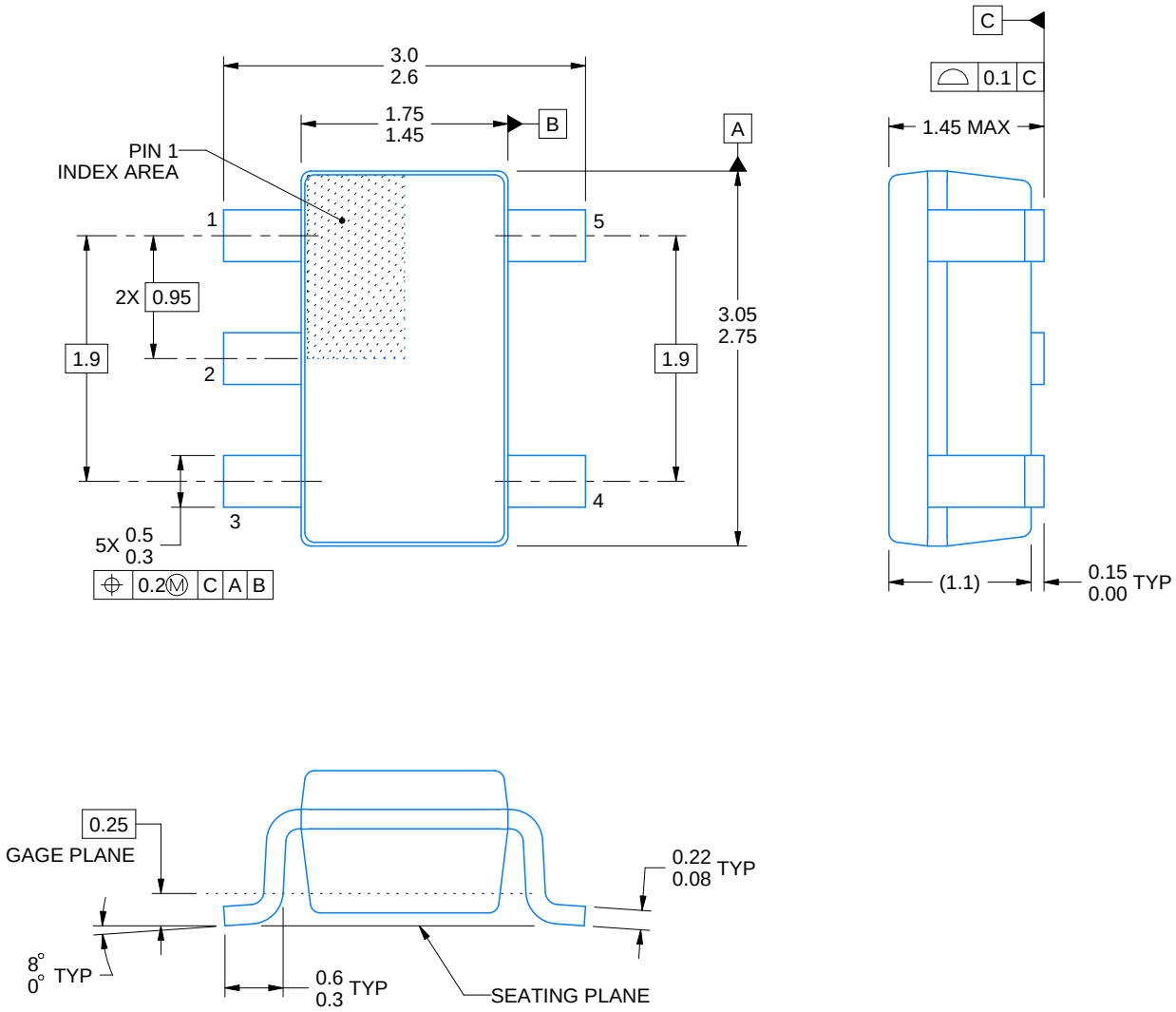
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

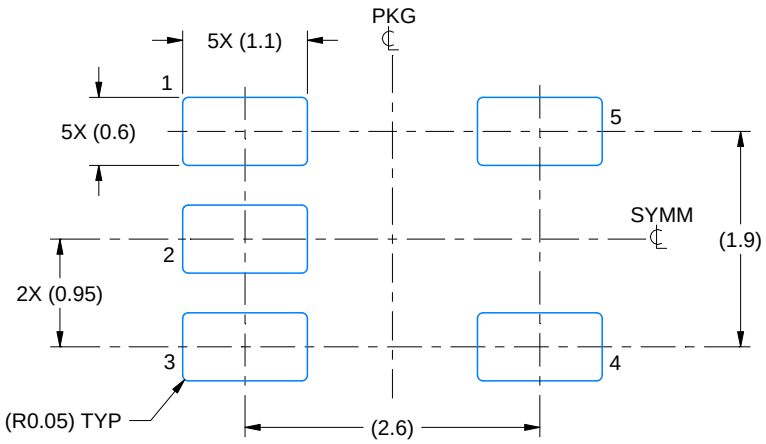
SMALL OUTLINE TRANSISTOR



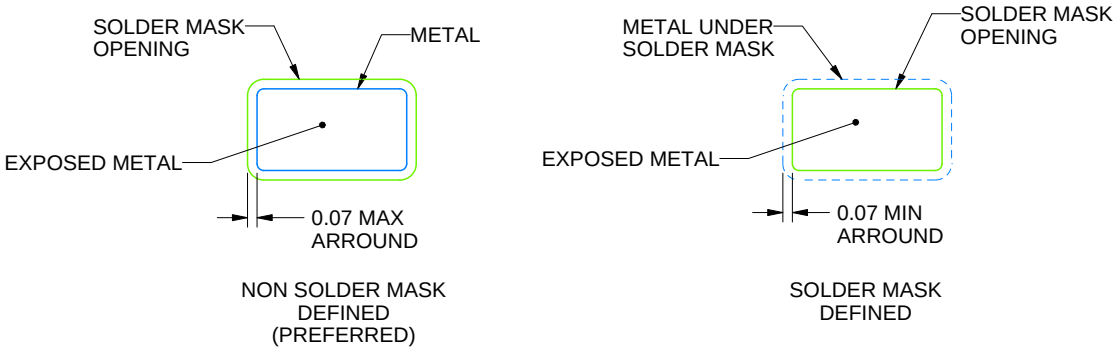
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

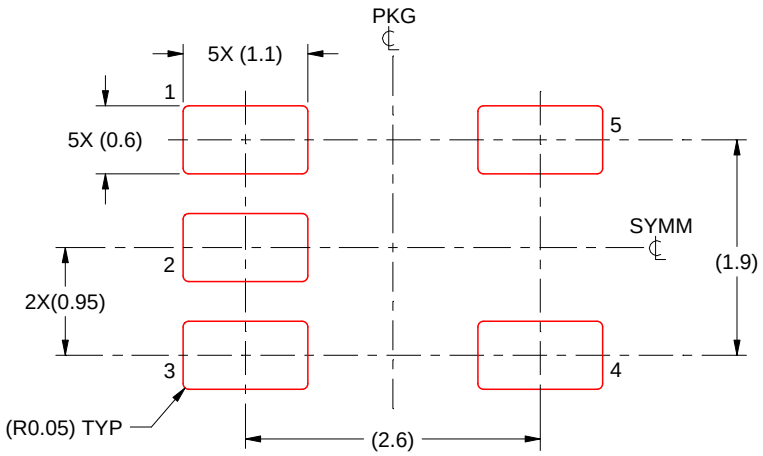


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

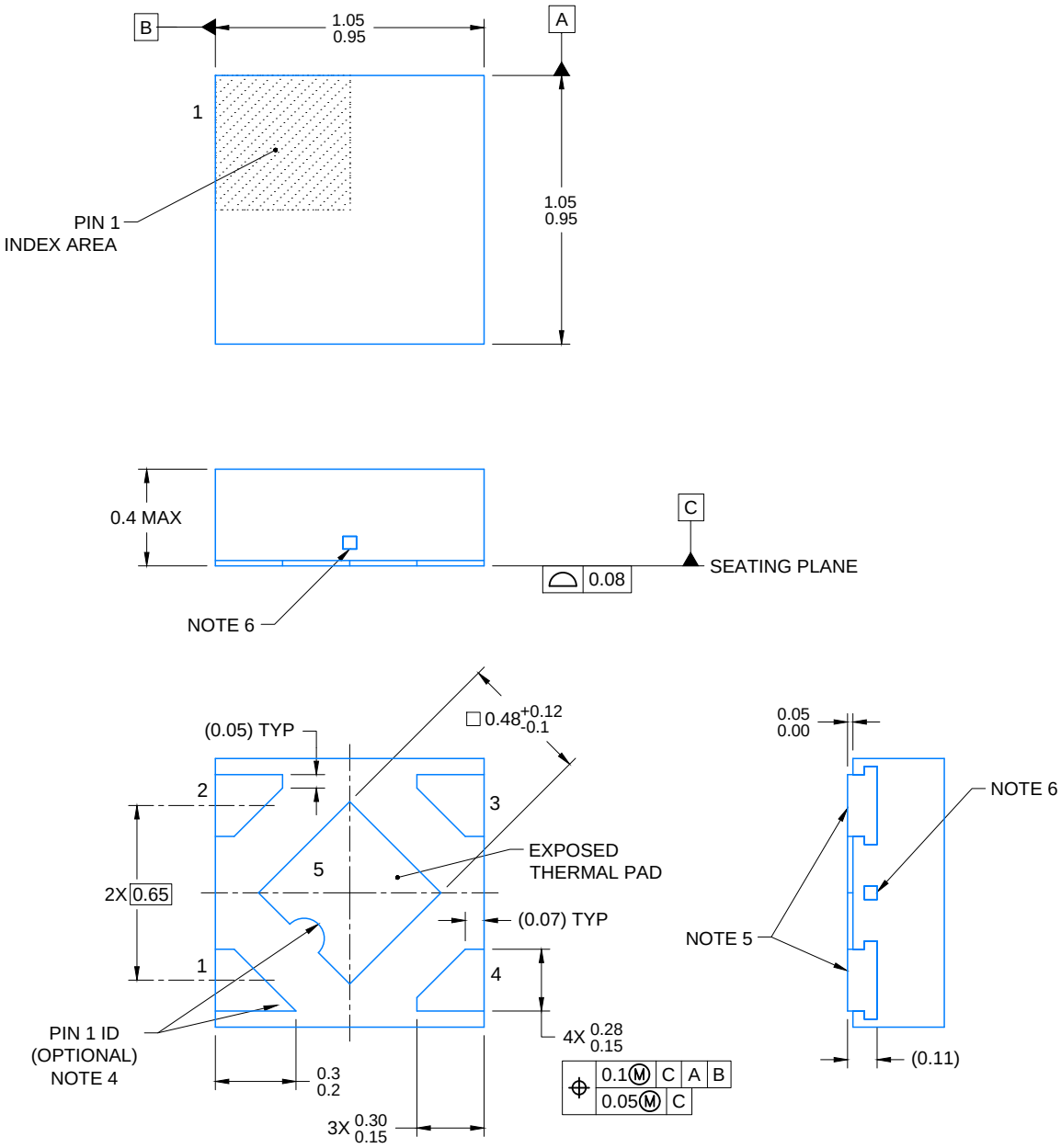
4210367/F

PACKAGE OUTLINE

DQN0004A

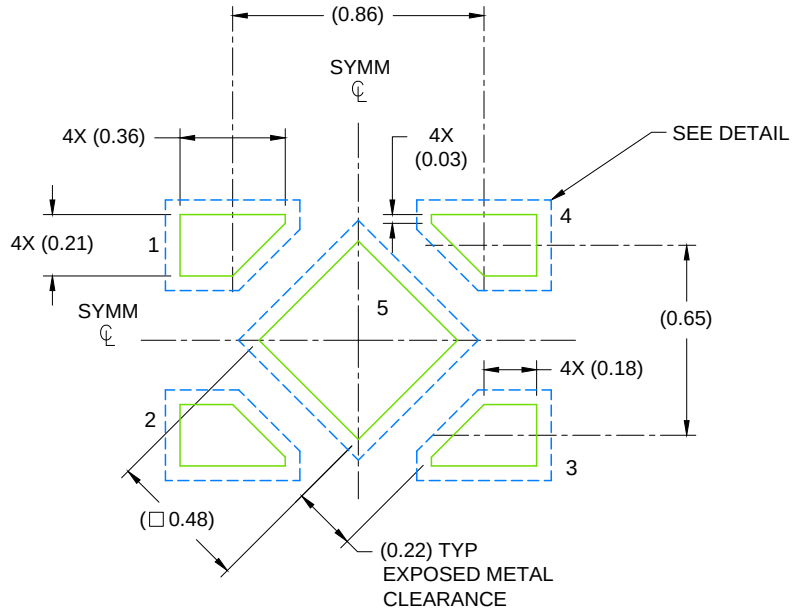
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



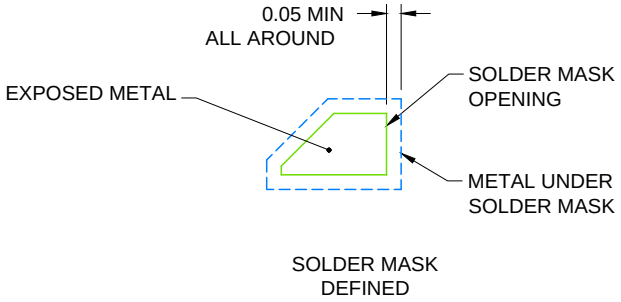
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE

SCALE: 40X

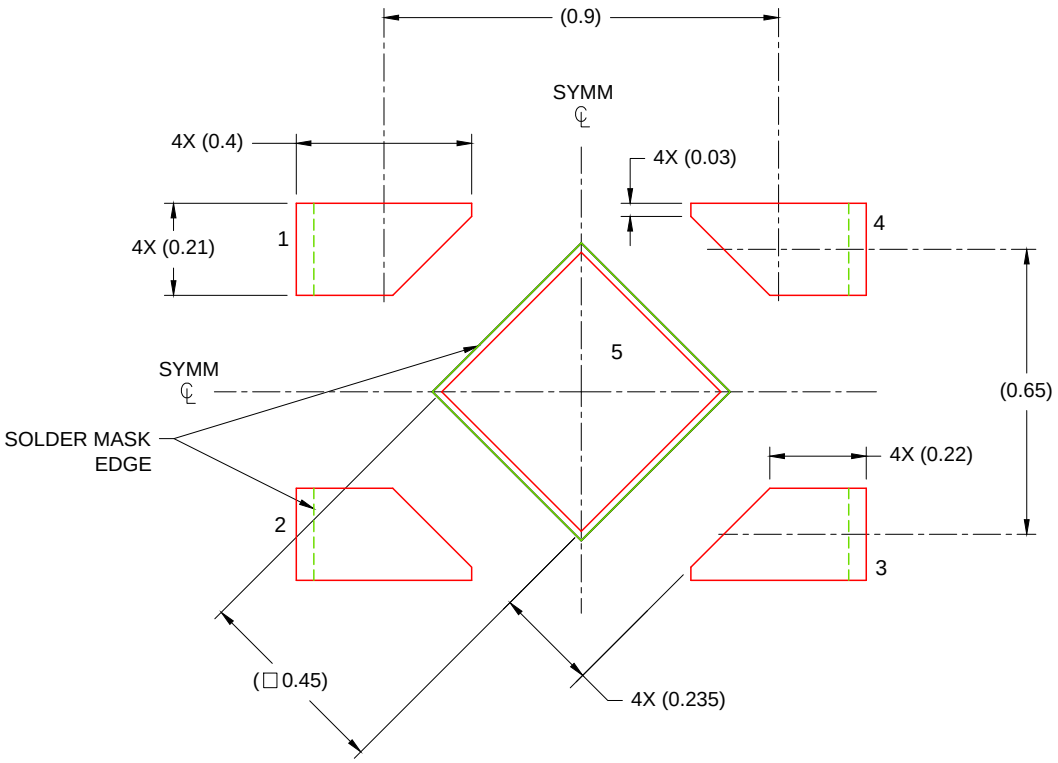


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

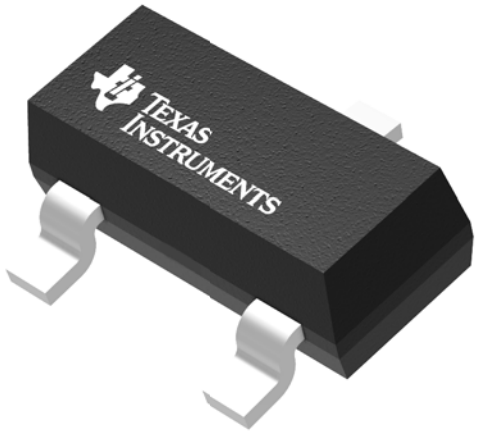
NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

DBZ 3 SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



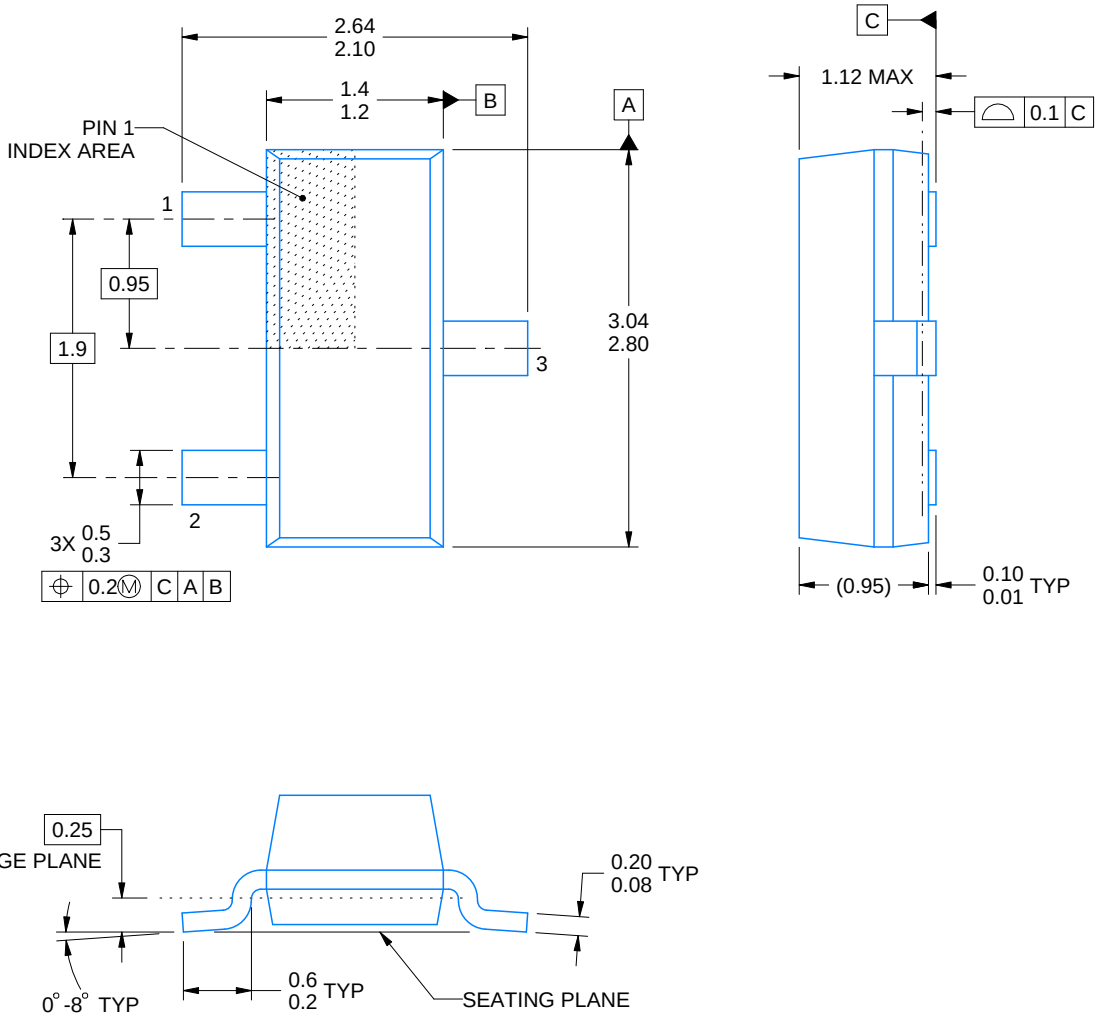
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

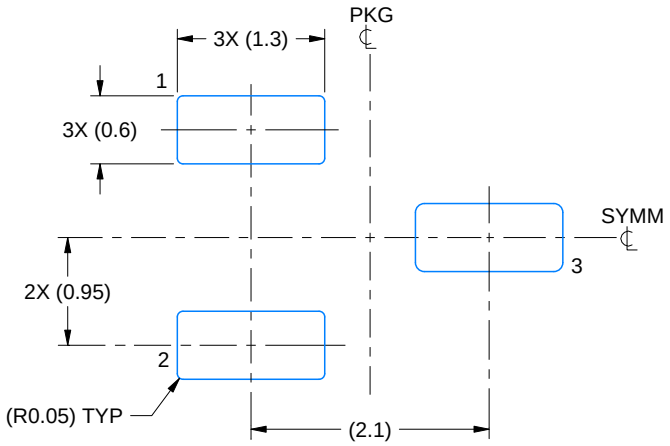
SMALL OUTLINE TRANSISTOR



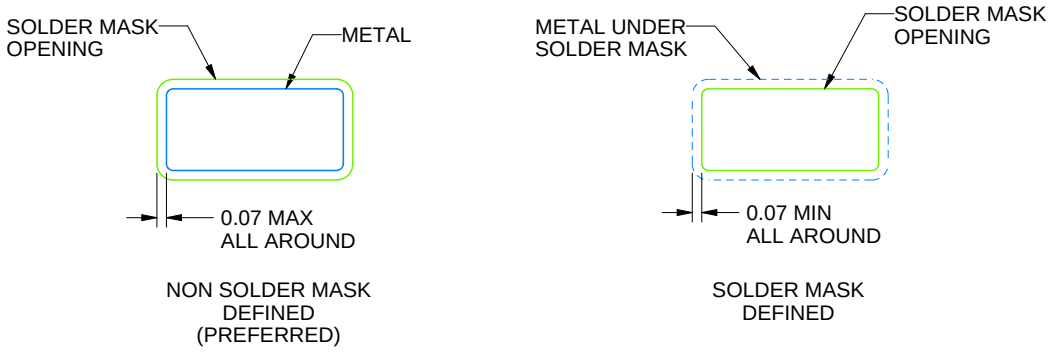
4214838/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.



LAND PATTERN EXAMPLE
SCALE:15X

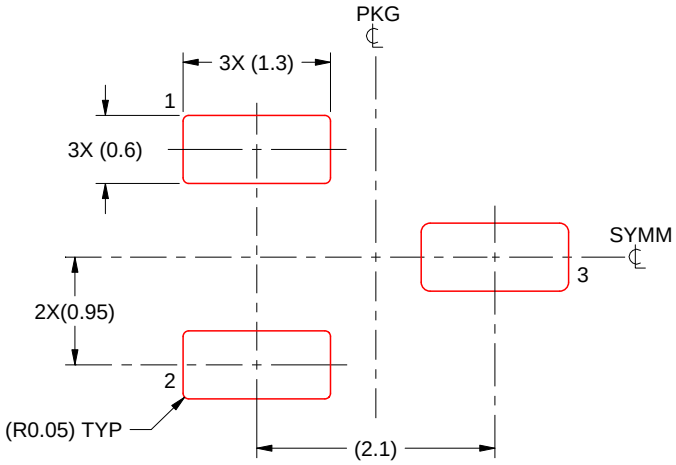


SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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