1. Arria II GX Device Family Overview

AIIGX51001-1.0

Introduction

The Arria® II GX device family is designed specifically for ease-of-use. The cost-optimized, 40-nm device family architecture features a low-power, programmable logic engine, and streamlined transceivers and I/Os. Common interfaces, such as the PCI Express (PIPE), Ethernet, and DDR-2 memory is easily implemented in your design with the Quartus® II software, SOPC Builder design software, Altera's broad library of hard-IP and soft-IP solutions. The Arria II GX device family makes designing for applications requiring transceivers operating at up to 3.75 Gbps fast and easy.

This chapter contains the following sections:

Highlights

The Arria II GX device features consist of the following highlights:

- 40 nm, low-power FPGA engine
  - Adaptive logic module (ALM) offers the highest logic efficiency in the industry
  - Eight-input fracturable look-up table (LUT)
  - Memory logic array blocks (MLABs) for efficient implementation of small FIFOs
- High-performance digital signal processing (DSP) blocks up to 350 MHz
  - Configurable as 9 × 9-bit, 12 × 12-bit, 18 × 18-bit, and 36 × 36-bit full precision multipliers
  - Hardcoded adders, subtractors, accumulators, and summation functions
  - Fully integrated design flow with MatLab and Altera's DSP Builder software
- Maximum system bandwidth
  - Up to 16 full-duplex clock data recovery (CDR)-based transceivers supporting rates between 155 Mbps and 3.75 Gbps
  - Dedicated circuitry to support physical layer functionality for popular serial protocols, including PCI Express (PIPE) Gen 1, Gigabit Ethernet, Serial RapidIO, Common Public Radio Interface (CPRI), Open Base Station Architecture Initiative (OBSAI), SD/HD/3G SDI, XAUI, HiGig/HiGig+, and SONET/SDH
- Complete PCI Express (PIPE) protocol solution with an embedded hard IP block that provides PHY-MAC layer, Data Link layer, and Transaction layer functionality

- Optimized for high-bandwidth system interfaces
  - Up to 612 user I/O pins arranged in up to 12 modular I/O banks that support a wide range of single-ended and differential I/O standards
  - High-speed LVDS I/O support with serializer/deserializer (SERDES) and dynamic phase alignment (DPA) circuitry at data rates from 150 Mbps to 1 Gbps
- Low power
  - Patented architectural power reduction techniques
  - Per-channel transceiver power consumption is approximately 100 mW under typical conditions at 3.125 Gbps
  - Power optimizations integrated into the Quartus II development software
- Advanced usability and security features
  - Parallel and serial configuration options
  - On-chip series and differential I/O termination
  - 256-bit advanced encryption standard (AES) programming file encryption for design security with volatile and non-volatile key storage options
  - Robust portfolio of IP for processing, serial protocols, and memory interfaces
  - Low cost, easy-to-use development kits featuring high-speed mezzanine connectors (HSMC)

Table 1–1 shows Arria II GX device features.

Table 1–1. Arria II GX Device Features (Part 1 of 2)

Feature	EP2AGX20	EP2AGX30	EP2AGX45	EP2AGX65	EP2AGX95	EP2AGX125	EP2AGX190	EP2AGX260
ALMs	6,380	10,800	18,050	25,300	37,470	49,640	76,120	102,600
LEs	15,950	27,000	45,125	63,250	93,675	124,100	190,300	256,500
PCI Express hard IP Blocks	1	1	1	1	1	1	1	1
M9K Blocks	87	144	319	495	612	730	840	950
Total Embedded Memory in M9K Blocks (Kbits)	783	1296	2871	4455	5508	6570	7560	8550
Total On-Chip Memory (M9K + MLABs) (Kbits)	982	1,634	3,435	5,246	6,679	8,121	9,939	11,756
Embedded Multipliers (18 × 18)	56	128	232	312	448	576	656	736
General Purpose PLLs	4	4	4	4	6	6	6	6
Transceiver Tx PLLs *(2)*	2	2	2 or 4 *(1)*	2 or 4 *(1)*	4 or 6 *(1)*	4 or 6 *(1)*	6 or 8 *(1)*	6 or 8 *(1)*

Table 1–1. Arria II GX Device Features (Part 2 of 2)

Feature	EP2AGX20	EP2AGX30	EP2AGX45	EP2AGX65	EP2AGX95	EP2AGX125	EP2AGX190	EP2AGX260
User I/O Banks	6	6	6	6	8	8	12	12

Notes to Table 1–1:

(1) The number of PLLs depends on package. Transceiver Tx PLL count = (number of transceiver blocks) × 2.

(2) The FPGA fabric can use these PLLs if they are not being used by the transceiver.

Table 1–2 lists Arria II GX device package options and user I/O pin counts, high-speed LVDS channel counts, and transceiver channel counts for micro BGA and FineLine BGA devices.

Table 1–2. Arria II GX Device Package Options and I/O Information *(Note 1)*, *(2)*

	358-Pin Flip Chip UBGA 17 mm × 17 mm			572-Pin Flip Chip FBGA 25 mm × 25 mm			780-Pin Flip Chip FBGA 29 mm × 29 mm			1152-Pin Flip Chip FBGA 35 mm × 35 mm		
Device	**I/O**	**LVDS *(3)***	**XCVRs**	**I/O**	**LVDS *(3)***	**XCVRs**	**I/O**	**LVDS *(3)***	**XCVRs**	**I/O**	**LVDS *(3)***	**XCVRs**
EP2AGX20	156	33Rx + 32Tx	4	252	57Rx + 56Tx	4	—	—	—	—	—	—
EP2AGX30	156	33Rx + 32Tx	4	252	57Rx + 56Tx	4	—	—	—	—	—	—
EP2AGX45	156	33Rx + 32Tx	4	252	57Rx + 56Tx	8	364	85Rx + 84Tx	8	—	—	—
EP2AGX65	156	33Rx + 32Tx	4	252	57Rx + 56Tx	8	364	85Rx + 84Tx	8	—	—	—
EP2AGX95	—	—	—	260	57Rx + 56Tx	8	372	85Rx + 84Tx	12	452	105Rx + 104Tx	12
EP2AGX125	—	—	—	260	57Rx + 56Tx	8	372	85Rx + 84Tx	12	452	105Rx + 104Tx	12
EP2AGX190	—	—	—	—	—	—	372	85Rx + 84Tx	12	612	145Rx + 144Tx	16
EP2AGX260	—	—	—	—	—	—	372	85Rx + 84Tx	12	612	145Rx + 144Tx	16

Notes to Table 1–2:

(1) The user I/O counts include clock pins.

(2) The arrows indicate packages vertical migration capability. Vertical migration allows you to migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

(3) Rx denotes LVDS input with OCT RD support or pseudo LVDS output. Tx denotes LVDS I/O without OCT RD support or pseudo LVDS output.

Arria II GX devices are available in up to three speed grades: –4 (fastest), –5, and –6 (slowest). Table 1–3 shows Arria II GX devices speed grades.

Table 1–3. Arria II GX FPGA Devices Speed Grades (Part 1 of 2)

Device	358-Pin Flip Chip UBGA	572-Pin Flip Chip FBGA	780-Pin Flip Chip FBGA	1152-Pin Flip Chip FBGA
EP2AGX20	C4, C5, C6, I5	C4, C5, C6, I5	—	—
EP2AGX30	C4, C5, C6, I5	C4, C5, C6, I5	—	—
EP2AGX45	C4, C5, C6, I5	C4, C5, C6, I5	C4, C5, C6, I5	—
EP2AGX65	C4, C5, C6, I5	C4, C5, C6, I5	C4, C5, C6, I5	—

Table 1–3. Arria II GX FPGA Devices Speed Grades (Part 2 of 2)

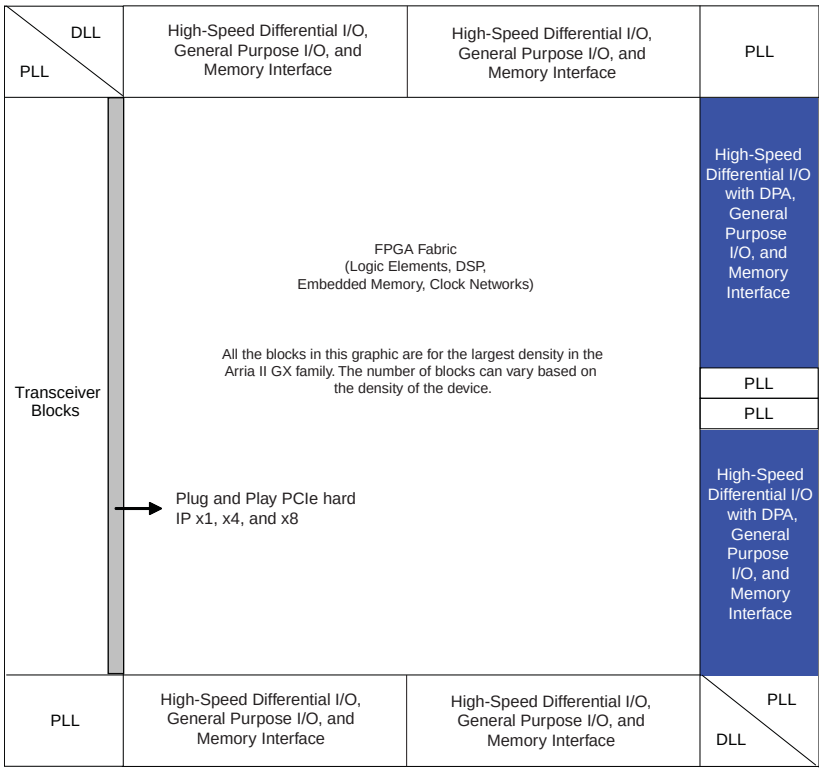
Device	358-Pin Flip Chip UBGA	572-Pin Flip Chip FBGA	780-Pin Flip Chip FBGA	1152-Pin Flip Chip FBGA
EP2AGX95	—	C4, C5, C6, I5	C4, C5, C6, I5	C4, C5, C6, I5
EP2AGX125	—	C4, C5, C6, I5	C4, C5, C6, I5	C4, C5, C6, I5
EP2AGX190	—	—	C4, C5, C6, I5	C4, C5, C6, I5
EP2AGX260	—	—	C4, C5, C6, I5	C4, C5, C6, I5

Arria II GX Device Architecture

Arria II GX FPGAs include a customer-defined feature set optimized for cost-sensitive applications and offer a wide range of density, memory, embedded multiplier, I/O, and packaging options. Arria II GX FPGAs support external memory interfaces and I/O protocols required by wireless, wireline, broadcast, computer, storage, and military markets. They inherit the 8-input advanced logic module, M9K embedded RAM block, and high-performance DSP blocks from the Stratix® IV device family with a cost-optimized I/O cell and a transceiver optimized for 3.75 Gbps speeds.

Figure 1–1 shows an overview of the Arria II GX device architecture.

Figure 1–1. Arria II GX Device Architecture Overview



High-Speed Transceiver Features

Arria II GX devices integrate up to 16 transceivers on a single device. The transceiver block is optimized for cost and power consumption. Arria II GX transceivers support the following features:

- Configurable pre-emphasis and equalization, and adjustable output differential voltage
- Flexible and easy-to-configure transceiver data path to implement proprietary protocols
- Signal Integrity Features
  - Programmable transmitter pre-emphasis to compensate for inter-symbol interference (ISI)
  - User-controlled five-stage receiver equalization with up to 7 dB of high-frequency gain
  - On-die power supply regulators for transmitter and receiver PLL charge pump and voltage-controlled oscillator (VCO) for superior noise immunity
  - Calibration circuitry for transmitter and receiver on-chip termination (OCT) resistors
- Diagnostic Features
  - Serial loopback from the transmitter serializer to the receiver CDR for transceiver PCS and PMA diagnostics
  - Parallel loopback from the transmitter PCS to the receiver PCS with built-in self test (BIST) pattern generator and verifier
  - Reverse serial loopback pre- and post-CDR to transmitter buffer for physical link diagnostics
  - Loopback master and slave capability in PCI Express hard IP blocks
  - Support for protocol features such as MSB-to-LSB transmission in SONET/SDH configuration and spread-spectrum clocking in PCI Express (PIPE) configuration

Table 1–4 shows some common protocols and the Arria II GX dedicated circuitry and features for implementing these protocols.

Table 1–4. Sample of supported Protocols and Feature Descriptions

Supported Protocols	Feature Descriptions

PCI Express (PIPE)	■ Complete PCI Express (PIPE) Gen1 protocol stack solution compliant to PCI Express Base Specification 1.1 that includes PHY-MAC, Data Link, and Transaction layer circuitry embedded in PCI Express hard IP blocks
	■ ×1, ×4, and ×8 lane configurations
	■ Built-in circuitry for electrical idle generation and detection, receiver detect, power state transitions, lane reversal, and polarity inversion
	■ 8B/10B encoder and decoder, receiver synchronization state machine, and ±300 parts per million (ppm) clock compensation circuitry
	■ Options to use:
	  ■ Hard IP Data Link Layer and Transaction Layer
	  ■ Hard IP Data Link Layer and custom Soft IP Transaction Layer

XAUI/HiGig/HiGig+	■ Compliant to IEEE P802.3ae specification ■ Embedded state machine circuitry to convert XGMII idle code groups (||I||) to and from idle ordered sets (||A||, ||K||, ||R||) at the transmitter and receiver, respectively ■ 8B/10B encoder and decoder, receiver synchronization state machine, lane deskew, and ±100 ppm clock compensation circuitry
GIGE	■ Compliant to IEEE 802.3 specification ■ Automatic idle ordered set (/I1/, /I2/) generation at the transmitter, depending on the current running disparity ■ 8B/10B encoder and decoder, receiver synchronization state machine, and 100 ppm clock compensation circuitry
CPRI/OBSAI	■ Reverse bit slipper eliminates latency uncertainty to comply with CPRI/OBSAI specifications ■ Optimized for power and cost for remote radio heads and RF modules

For other protocols supported by Arria II GX devices, such as SONET/SDH, SDI and Serial RapidIO, refer to the *Arria II GX Transceiver Architecture* chapter in volume 2 of the *Arria II GX Device Handbook*.

The following sections provide an overview of the various features of the Arria II GX FPGA.

PCI Express (PIPE) hard IP

Every Arria II GX device includes an integrated hard IP block which implements PCI Express (PIPE) PHY-MAC, data link, and transaction layers. This PCI Express hard IP block is highly configurable to meet the requirements of the majority of PCI Express applications. PCI Express (PIPE) hard IP makes implementing a PCI Express (PIPE) Gen 1 solution in your Arria II GX design simple and easy.

PCI Express hard IP is instantiated using the PCI Compiler MegaWizard™ Plug-In Manager, similar to soft IP functions, but does not consume core FPGA resources or require placement, routing, and timing analysis to insure correct operation of the core. The Arria II GX hard IP for PCI Express (PIPE) includes support for:

- ×1, ×4, and ×8 lane configurations
- Root port and endpoint configurations
- 512 byte payload
- Compliant to PCI Express (PIPE) 1.1 at 2.5 Gbps

Logic Array Block and Adaptive Logic Modules

- Logic array blocks (LABs) consists of 10 adaptive logic modules (ALMs), carry chains, shared arithmetic chains, LAB control signals, local interconnect, and register chain connection lines
- ALMs expand the traditional four-input LUT architecture to eight-inputs, increasing performance by reducing LEs, logic levels, and associated routing
- LABs have a derivative called memory LAB (MLAB), that adds SRAM-memory capability to the LAB
- MLAB and LAB blocks always coexist as pairs, allowing up to 50% of the logic (LABs) to be traded for memory (MLABs)

Embedded Memory Blocks

- M9K embedded memory blocks provide up to 8,550 Kbits of on-chip memory capable of up to 390-MHz performance. The embedded memory structure consists of columns of M9K memory blocks that you can configure as RAM, FIFO buffers, and ROM
- Optimized for applications such as high-throughput packet processing, high-definition (HD) line buffers for video processing functions, and embedded processor program and data storage
- Quartus II software allows you to take advantage of M9K memory blocks by instantiating memory using a dedicated megafunction wizard or by inferring memory directly from VHDL or Verilog source code

Table 1–5 shows Arria II GX device memory modes.

Table 1–5. Arria II GX Memory Modes

Port Mode	Port Width Configuration
Single Port	×1, ×2, ×4, ×8, ×9, ×16, ×18, ×32, and ×36
Simple Dual Port	×1, ×2, ×4, ×8, ×9, ×16, ×18, ×32, and ×36
True Dual Port	×1, ×2, ×4, ×8, ×9, ×16, and ×18

DSP Resources

- Fulfills the digital signal processing requirements of 3G and LTE wireless infrastructure applications, video processing applications, and voice processing applications
- DSP block input registers efficiently implement shift registers for finite impulse response (FIR) filter applications
- Quartus II software includes megafunctions that are used to control the mode of operation of the DSP blocks based on user-parameter settings
- Multipliers can also be inferred directly from VHDL or Verilog HDL source code

I/O Features

- Contains up to 12 modular I/O banks
- All I/O banks support a wide range of single-ended and differential I/O standards, as listed in Table 1–6

Table 1–6. Arria II GX FPGA I/O Standards Support

Type	I/O Standard
Single-Ended I/O	LVTTL, LVCMOS, SSTL, HSTL, PCI, and PCI-X
Differential I/O	SSTL, HSTL, LVPECL, LVDS, mini-LVDS, and RSDS

- Supports programmable bus hold, programmable weak pull-up resistors, and programmable slew rate control
- Calibrates OCT or driver impedance matching for single-ended I/O standards with one OCT calibration block on the top-left, top-right, and bottom-left corners of the device
- Dedicated configuration banks at Bank 3C and 8C which support dedicated configuration pins and dual-function pins with a configuration scheme at 1.8, 2.5, 3.0, and 3.3 V
- Dedicated V_{REF} pin per I/O bank to allow voltage-referenced I/O standards. Each I/O bank can operate at independent V_{CCIO} and V_{REF} levels

High-Speed LVDS I/O with DPA and Soft CDR

- Dedicated circuitry for implementing LVDS interfaces at speeds from 150 Mbps to 1 Gbps
- On-chip differential termination for high-speed LVDS interfacing
- DPA circuitry and soft-CDR circuitry at the receiver automatically compensates for channel-to-channel and channel-to-clock skew in source-synchronous interfaces and allows for implementation of asynchronous serial interfaces with embedded clocks at data rates from 150 Mbps to 1 Gbps

Clock Management

- Provides dedicated global clock networks (GCLKs), regional clock networks (RCLKs), and periphery clock networks (PCLKs) that are organized into a hierarchical structure that provides up to 148 unique clock domains
- Up to six PLLs with seven outputs per PLL to provide robust clock management and synthesis
  - Independently programmable PLL outputs, creating a unique and customizable clock frequency with no fixed relation to any other clock
  - Inherent jitter filtration and fine granularity control over multiply and divide ratios
  - Supports spread-spectrum input clocking and counter cascading with PLL input clock frequencies ranging from 5 to 500 MHz to support both low-cost and high-end clock performance
- Unused transceiver PLLs can be used by the FPGA fabric to provide more flexibility

Auto-Calibrating External Memory Interfaces

- I/O structure enhanced to provide flexible and cost-effective support for different types of memory interfaces
- Contains features such as on-chip termination and DQS/DQ pin groupings to enable rapid and robust implementation of different memory standards
- An auto-calibrating megafunction is available in the Quartus II software for DDR SDRAM, DDR2 SDRAM, and DDR3 SDRAM memory interface PHYs; the megafunction takes advantage of the PLL dynamic reconfiguration feature to calibrate based on the changes of process, voltage, and temperature

Table 1–7 lists preliminary external memory support. Memory maximum performance is pending device characterization.

Table 1–7. Arria II GX Device External Memory Interface Maximum Performance

Memory Type	Maximum Performance
DDR SDRAM	200 MHz
DDR2 SDRAM	300 MHz
DDR3 SDRAM	300 MHz
QDRII SRAM	250 MHz

Arria II GX devices feature I/O capable of electrical support for QDRII SRAM, but Altera does not currently supply a controller or PHY megafunction for QDRII SRAM interfaces.

For more information regarding the external memory interfaces support, refer to the *External Memory Interfaces in Arria II GX Devices* chapter in volume 1 in the *Arria II GX Device Handbook*.

Nios II

- Arria II GX devices support all variants of the NIOS II processor
- Nios II processors are supported by an array of software tools from Altera and leading embedded partners and are used by more designers than any other configurable processor

Configuration Features

- Configuration
  - Meets the 200 ms wake-up time requirement for PCI Express (PIPE)
- Design Security
  - Supports programming file encryption using 256-bit volatile and non-volatile security keys to protect designs from copying, reverse engineering, and tampering in fast passive parallel (FPP) configuration mode with an external host (such as a MAX® II device or microprocessor), or when using fast active serial (AS) or passive serial (PS) configuration scheme
  - Decrypts an encrypted configuration bitstream using the AES algorithm, an industry standard encryption algorithm that is FIPS-197 certified and requires a 256-bit security key
- Remote System Upgrade
  - Allows error-free deployment of system upgrades from a remote location securely and reliably without an external controller
  - Soft logic (either the Nios II embedded processor or user logic) implementation in the device helps download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to start a reconfiguration cycle
  - Dedicated circuitry in the remote system upgrade helps to avoid system down time by performing error detection during and after the configuration process, and recover from an error condition by reverting back to a safe configuration image, and provides error status information

SEU Mitigation

- Offers built-in error detection circuitry to detect data corruption due to soft errors in the configuration random access memory (CRAM) cells
- Allows all CRAM contents to be read and verified to match a configuration-computed cyclical redundancy check (CRC) value
- The bit location and the type of soft error can be identified and read-out through the Joint Test Action Group (JTAG) or the core interface

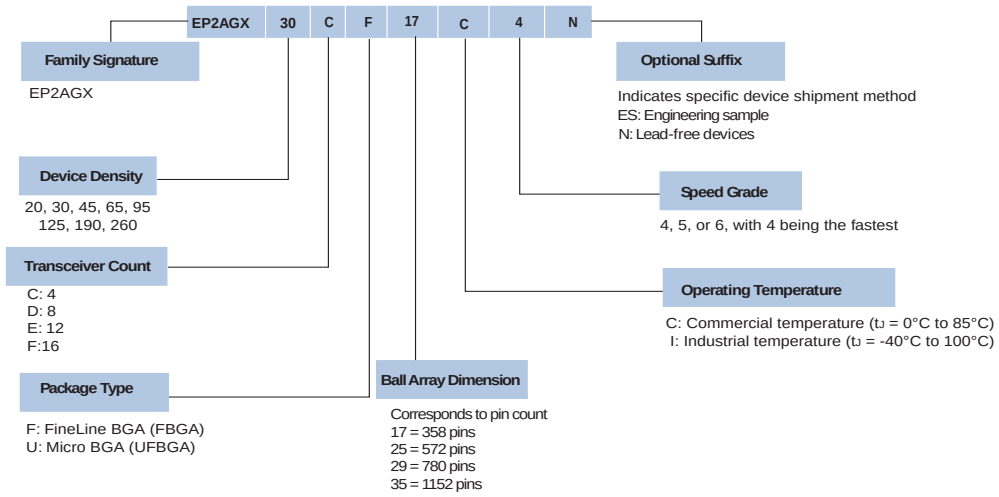
JTAG Boundary Scan Testing

- Supports JTAG IEEE Std. 1149.1 and IEEE Std. 1149.6 specifications
- IEEE Std. 1149.6 supports high-speed serial interface (HSSI) transceivers and performs boundary scan on alternating current (AC)-coupled transceiver channels
- Boundary-scan test (BST) architecture offers the capability to test pin connections without using physical test probes and capture functional data while a device is operating normally

Reference and Ordering Information

Figure 1–2 describes the ordering codes for Arria II GX devices.

Figure 1–2. Arria II GX Device Packaging Ordering Information



Document Revision History

Table 1–8 shows the revision history for this document.

Table 1–8. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
February 2009, v1.0	Initial Release.	—