## Cyclone III LS FPGAs

## Introducing Cyclone III LS Devices

- Low power
- 200K LE for under 0.25 Watt
- TSMC 60-nm low-power (LP) process
- Quartus II software power-aware design flow
- Information assurance design capabilities
- Anti-tamper
- Design security
- Design separation
- IP, design examples, etc.
- High functionality
- Densities ranging from 70K to 200K LEs
- Up to 8 Mbits of embedded memory
- Up to 396 embedded multipliers



## High-Functionality AND Low-Power Solution

- Increase processing bandwidth and lower power
- 200K logic elements, 8.2 Mbits of embedded RAM, and $39618 \times 18$ multipliers for less than 0.25 Watt static power
- Increase energy efficiency or extend battery life
- Cyclone III LS FPGAs have the market's lowest power profile
- Jump-start new designs using reference examples
- Re-use Altera's Video and Image Processing (VIP) Suite: IP, kits, and reference designs
- Protect IP investments in new products
- Cyclone III LS FPGAs enable hardware-based security


## Cyclone II/ LS FPGA provides DSP and data processing AND low power

## Extending Low-Power Leadership



## Double the resources for less than 0.25 Watt

## At $85^{\circ} \mathrm{C}$ junction temperature

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## The Value of Security Features

■ "...estimated competing gray market sales cost the company between $\$ 200$ and $\$ 300$ Million in lost revenue during FY 2006."

■ "One out of every ten IT products contains counterfeit semiconductors."

## Security critical for revenue and brand image

[^0]5

## Protect IP With Anti-Tamper and Design Security



## The most comprehensive IP protection in an FPGA

## Design Separation Feature



## Benefits

Example design requirements

- Redundancy required for high up-time and reliability
- Easily design single chip redundancy and information assurance applications
- Reduce board complexity



## Data Assurance With Design Separation Feature



- Physically isolated partitions with design separation
- Protect against time-dependent faults and SEU
- Increase system up-time
- Achieve a higher level of integration on a single device


## Example - Video and Image Processing Trends



## Video and imaging application examples

- Medical/industrial/military imaging
- Video surveillance
- Video conferencing

High functionality ...... • Video standards continue to evolve, driving higher data rates (e.g. H.264)

- Processing requirements are outpacing DSP performance

Lower R\&D \$

- ASIC design cycles do not meet time-to-market needs
- Frequently require re-spins and sizable NRE
- Extending battery life or increasing energy efficiency

Lower power

- Thermal dissipation can interfere with sensitive CCD image capture devices


## Example - Industrial Trends

- Standardization of Industrial Ethernet (IE) protocols
- FPGA supports all IE protocols with one hardware platform
- Energy efficiency
- FPGA enables cost-effective variable motion control solutions, increasing efficiency by up to $85 \%$
- Secure IP for revenue protection
- The most comprehensive IP protection in an FPGA
- Long product life cycles
- Obsolescence-proof to avoid costly re-designs

[^1]10

## Redundancy in Industrial Motor Control

## Cyclone III FPGA



## Cyclone III LS FPGA



- Reduce board space by up to $50 \%$ with design separation
- Reduce BOM cost with integration
- Secure IP with anti-tamper and design security

[^2]
## Example - Military Market Trends

- Size, weight, and power (SWaP)
- Support next-generation software-defined radio (SDR) waveforms with small footprint and low power, e.g. MUOS, SRW
- Night-vision goggles
- Secure communications
- Crypto modernization moving towards standardization
- Interoperability
- Common criteria for equipment in US, Canada, and Europe - NIST, FIPS, IPsec
- COTS
- Reduce cost
- Reduce time to market
- Increased product life cycle with COTS products


## Existing SDR Application



- Next-generation SDR waverforms require:
- More memory and logic resources for networking in the field
- Low power for extended battery life
- Small footprint for board space
- Data security
- IP security and anti-tamper


## Next Generation SDR



- Reduce board space by up to $50 \%$
- Increase battery life by up to 2 X
- Single-chip secure SDR solution

[^3]
## Cyclone III LS FPGAs - Device Resources

| Product line | LEs | Memory (Mbits) |  | $18 \times 18$ multipliers | PLLs | Global clocks | Static power* (mW) | Security features |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| EP3CLS70 | 70,208 | 3.1 | 333 | 200 | 4 | 20 | 164 |  |
| EP3CLS100 | 100,488 | 4.5 | 483 | 276 | 4 | 20 | 170 |  |
| EP3CLS150 | 150,848 | 6.1 | 666 | 320 | 4 | 20 | 233 |  |
| EP3CLS200* | 198,464 | 8.2 | 891 | 396 | 4 | 20 | 245 |  |


| Core <br> (MHz) | Memory <br> (MHz) | Multipliers <br> (MHz) | LVDS <br> (Mbps) | DDR / DDR2 <br> (Mbps) | QDR II <br> (Mbps) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 402 | 238 | 200 | 640 | 333 | 600 |

Performance shown for slowest speed grade (C8)

[^4]
## Device Packaging and I/O Matrix

| Product line | U484 <br> 0.8 mm <br> $19 \times 19$ |  | F484 <br> 1.0 mm <br> $23 \times 23$ |  | F780 <br> 1.0 mm <br> $29 \times 29$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1/0 | LVDS | 1/0 | LVDS | I/O | LVDS |
| EP3CLS70 | 278 | 78 | 278 | 78 | 413 | 177 |
| EP3CLS100 | -278 | -78 | 278 | 78 | 413 | 177 |
| EP3CLS150 | - | - | 210 | 78 | 413 | 177 |
| EP3CLS200 | - | - | 210 | 78 | 413 | 177 |



## Highest density + smallest package

Commercial ( $-7,-8$ ) and industrial (-i7) speed grades supported

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## Cyclone III LS Key Architectural Features



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## Cyclone III LS FPGAs - Rollout Schedule

| Device | General <br> rollout | Commercial <br> -7 | Industrial <br> -7 | Commercial <br> -8 |
| :---: | :---: | :---: | :---: | :---: |
| EP3CLS200 | June 2009 - ES <br> 4Q 2009 - Production | 4Q 2009 | 4Q 2009 | F484 - July <br> F780 - Aug. |
| EP3CLS150 | 4Q 2009 | Dec. 2009 | Dec. 2009 | Nov. 2009 |
| EP3CLS100 | 1Q 2010 | 1 1Q 2010 |  |  |
| EP3CLS70 | 2Q 2010 |  |  |  |

## Now shipping

[^7]
## Cyclone III LS FPGA Dev Kit



## Shipments begin Sept. - Oct. 2009

[^8]

## Summary

- The most comprehensive IP protection in an FPGA
- Anti-tamper to prevent cloning or counterfeiting
- Design security using state-of-the-art 256-bit AES
- Design separation for information assurance
- Design examples to jump-start your design
- The FPGA industry's most efficient low-power devices per density and package size
- 200K LE density for under 0.25 Watt (static power)
- 100K LE density in $19 \times 19 \mathrm{~mm}$ and 200 K LE in $23 \times 23 \mathrm{~mm}$
- Increased data and imaging processing
- 100\% more on-chip memory
- $80 \%$ more on-chip multipliers
- FPGAs and software shipping now


[^0]:    Sources: New Momentum White Papers (http://www.newmo.com/downloads.html)
    "Fighting High Tech Counterfeiting with High Tech Solutions" and "Intellectual Property Fraud Prevention"
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[^1]:    Source: SIA
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[^4]:    * Pstatic from EPE, junction temperature $=85^{\circ} \mathrm{C}$
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