Cyclone III FPGA Family

Unprecedented combination of low power, high functionality, and low cost to enable your new designs

Meeting the Needs of Emerging High-Volume Applications

- *2 – 20K logic elements (LEs)*
- *295-Kbits embedded RAM*
- *DDR support*
- *Nios® embedded processor*

2002

- *5 – 70K LEs*
- *1.1-Mbits embedded RAM*
- *150 18 x 18 multipliers for DSP*
- *DDR2 support*
- *Nios II embedded processor*

2004

- *50% lower power vs. Cyclone® II FPGAs*
- *5 – 120K LEs*
- *4-Mbits embedded RAM*
- *288 18 x 18 multipliers for DSP*
- *Higher performance DDR2 support*
- *Nios II embedded processor*

2007

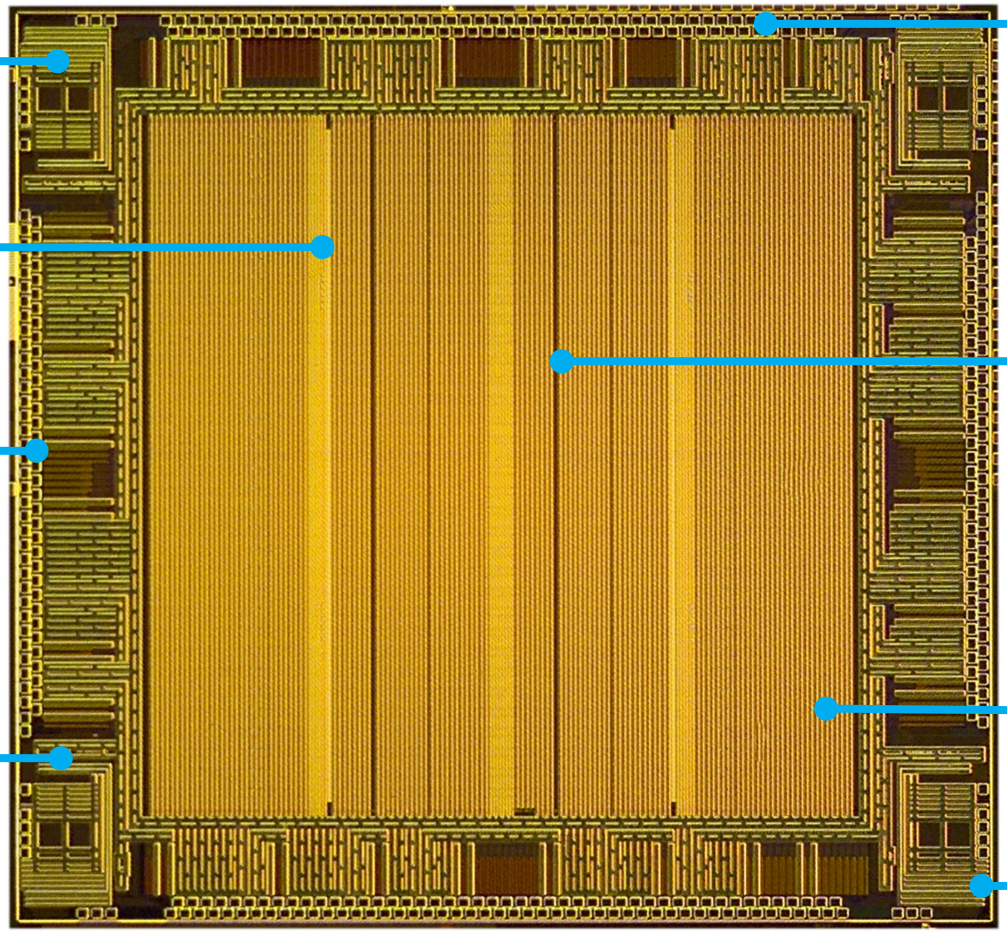
Cyclone III Key Architectural Features

65-nm low-power process

Up to 4-Mbit embedded memory

Up to 535 flexible user I/O pins

Parallel and serial configuration with new remote update feature



400-Mbps external memory interfaces

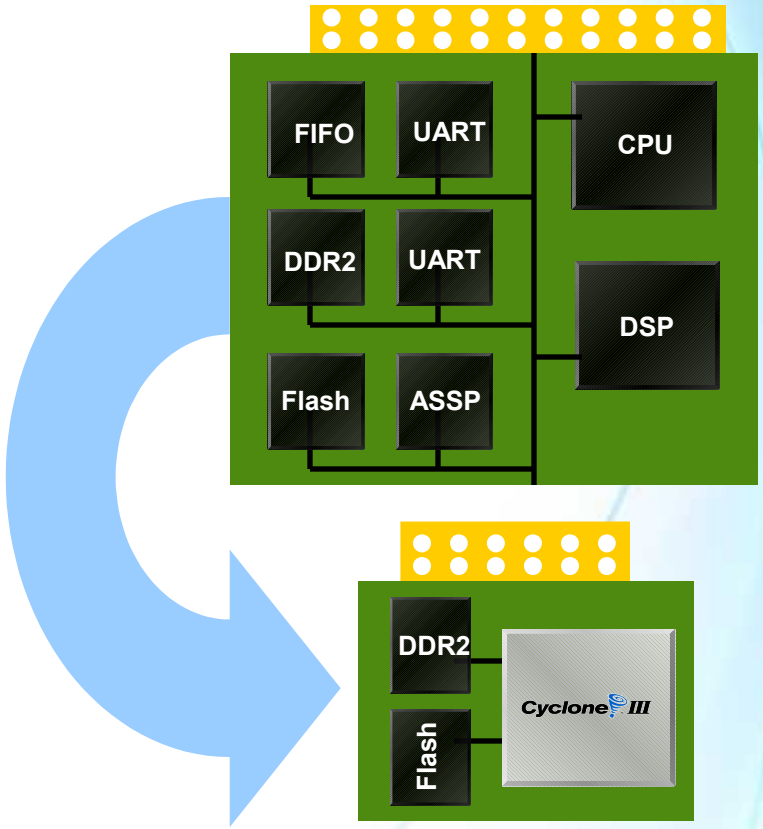
Up to 288 embedded multipliers for high-throughput DSP

5 – 120K LEs

Dynamically configurable phase-locked loops (PLLs)

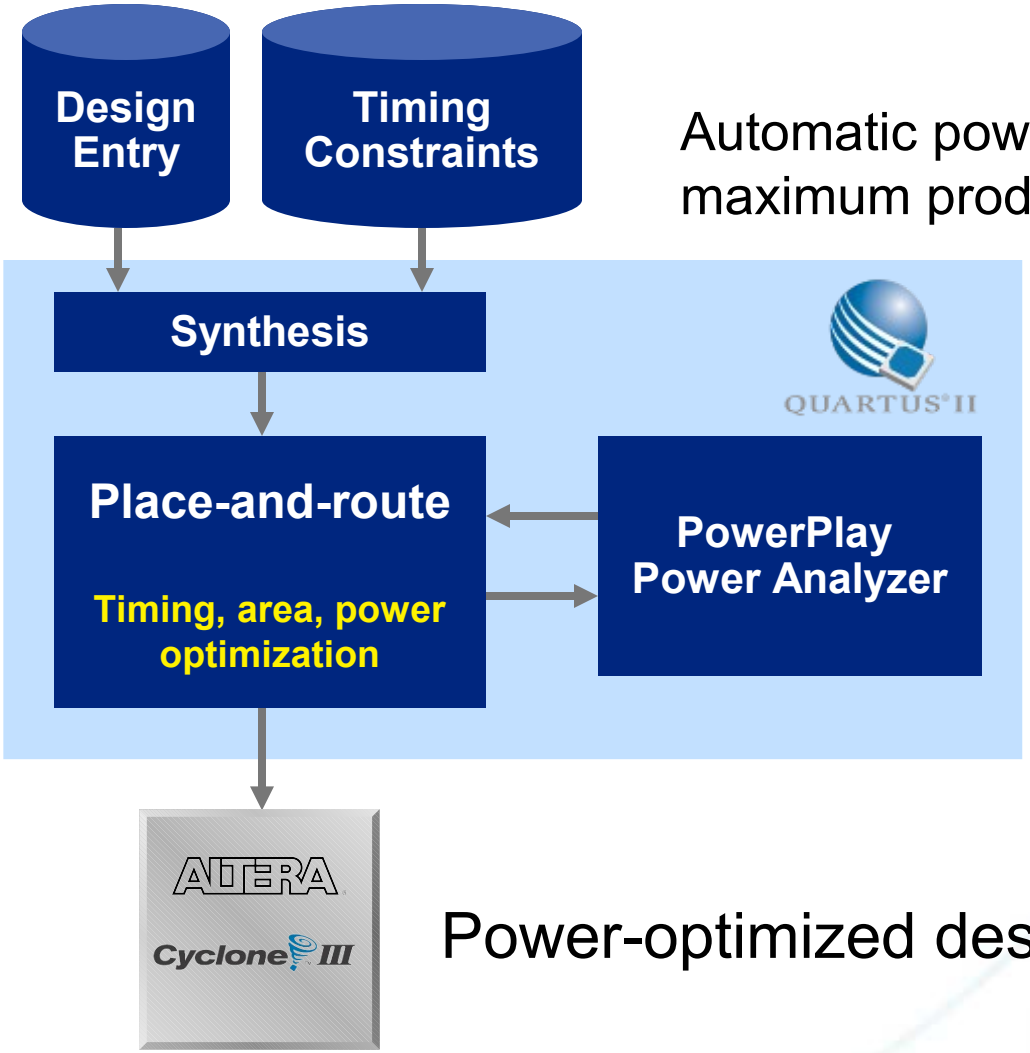
System Integration

- System integration eases your design constraints
  - Board space requirements
  - Cost pressures
  - Product obsolescence concerns
  - Short development times
- Cyclone III FPGAs—complete feature set for better integration over any other low-cost FPGA



Do more with less!

Power-Aware Design With Quartus II Software



Automatic power reduction for maximum productivity

Up to 25% lower power

Power-optimized design ☑

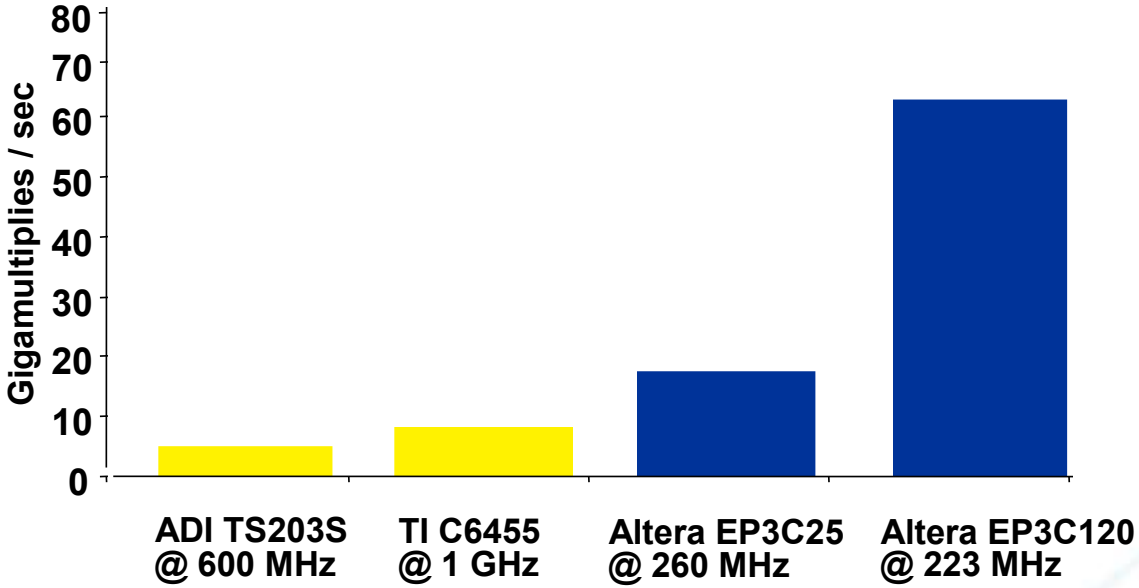
Lowest-Power Low-Cost FPGAs

Cyclone III family power reduction technique	Lower static power	Lower dynamic power
Process optimization	✓	✓
Power-aware design with Quartus II software		✓

50+ Percent Power Reduction vs. Cyclone II FPGAs

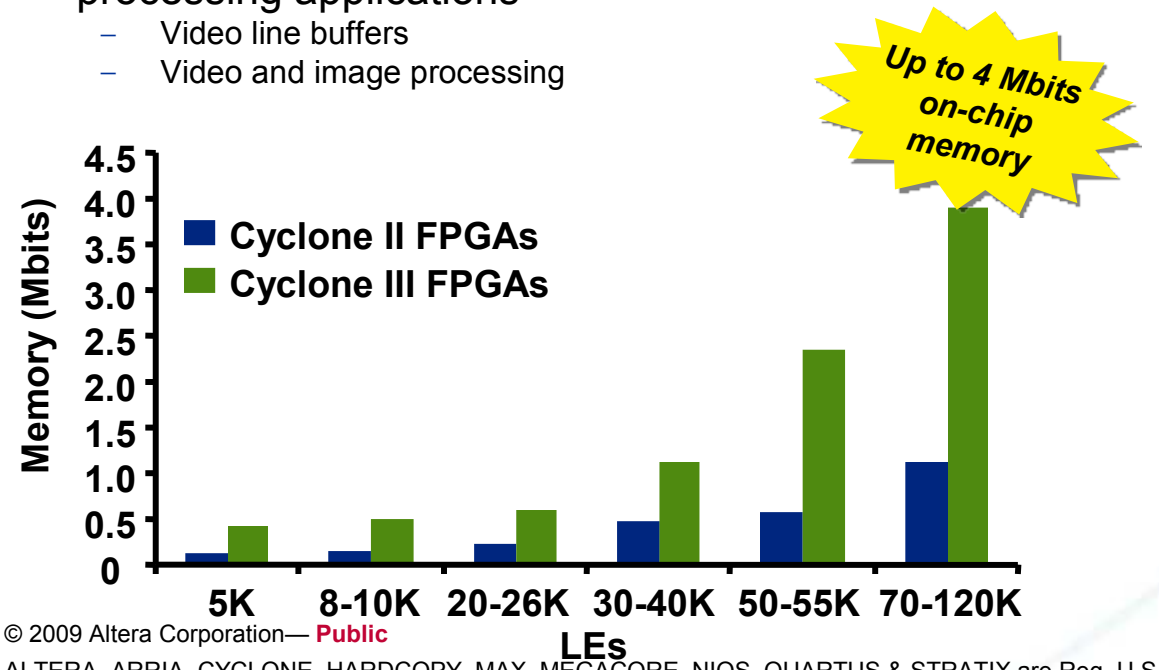
DSP Advantages

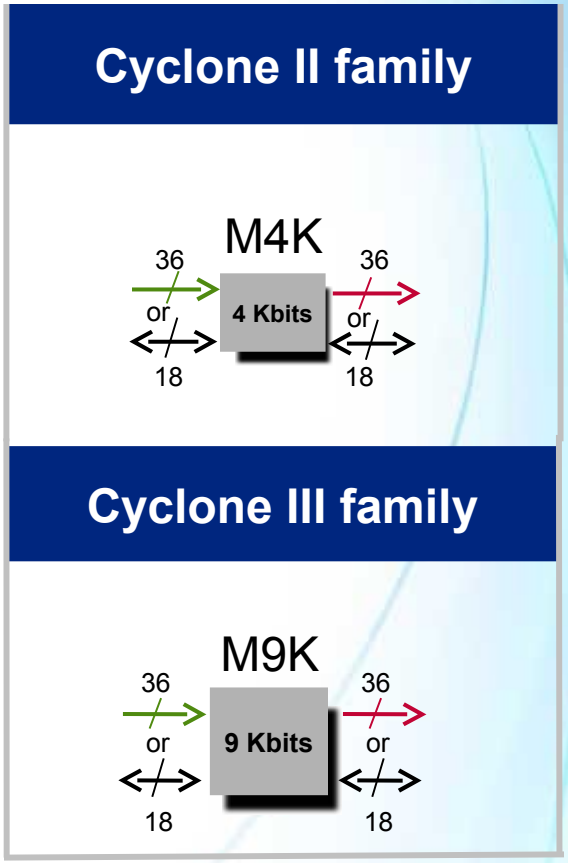
- Combination of logic, memory, and multipliers allows for efficient implementation of arithmetic DSP functions
  - Integrate multiple DSP devices into a single Cyclone III FPGA
  - Process multiple signal data streams at lower cost per channel than dedicated DSP devices



Memory Optimizations

- Increased memory block size
  - Allows for increased memory capacity
- Higher memory-to-logic ratio
  - Implement packet buffers
  - Integrate larger data and instruction caches for embedded processors
  - Integrate larger FIFO buffers
- Optimized memory-to-multiplier ratio for intensive processing applications
  - Video line buffers
  - Video and image processing

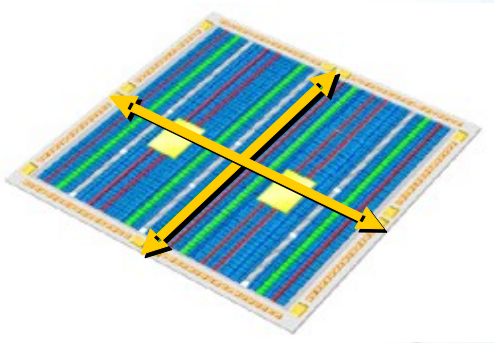




Clocking Resources

- Clock routing resources
  - Up to 20 global clocks
  - Global clock routing can also be used for global signals
  - Powered down when not in use to save power
- Full-featured and robust PLLs
  - Up to four low-jitter (200 ps) PLLs
  - Five programmable outputs per PLL
  - Wide frequency range of 5 to 440 MHz
  - Dynamically change both frequency and phase
  - Cascadable to allow broader frequency generation

Global clock networks



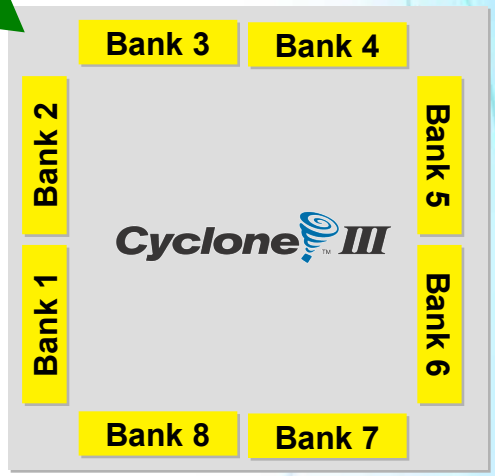
Up to 20 networks per device

Flexible and robust clocking resources to support higher system integration

I/O Pin Features

- Variety of I/O Standards
  - HSTL, SSTL Class I and II
  - LVDS, RSDS, Mini-LVDS, PPDS
  - LVCMOS
  - LVTTL
  - LVPECL
  - PCI, PCI-X
- 3.3-V compatible
- On-chip termination
- Adjustable slew rates
- Eight banks of every device in the family
  - Each can implement any supported I/O standard
- Dedicated memory interfaces
  - QDR II, DDR, and DDR2

LVDS up to 875 Mbps

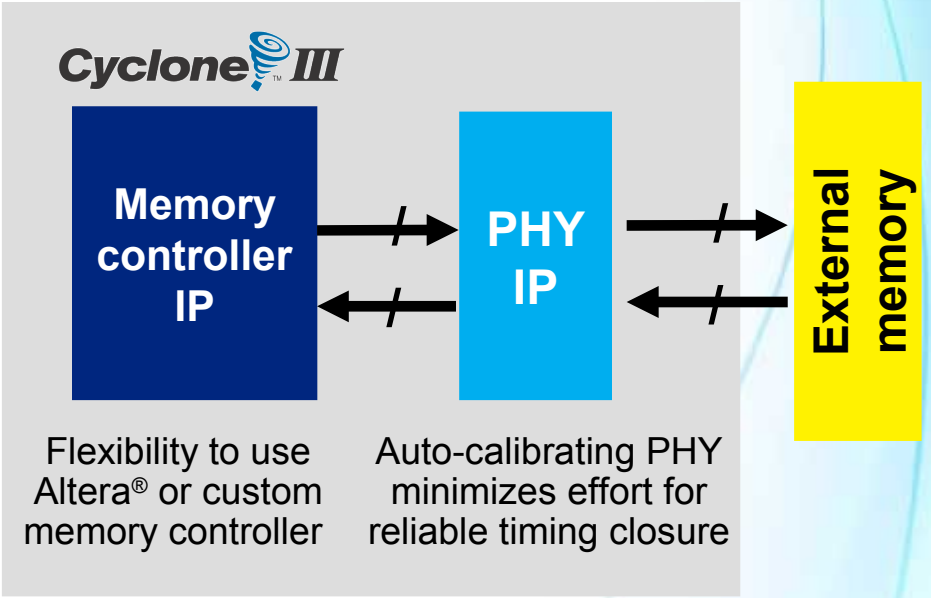


DDR2 up to 400 Mbps

Complete flexibility to implement a wide variety of I/O standards

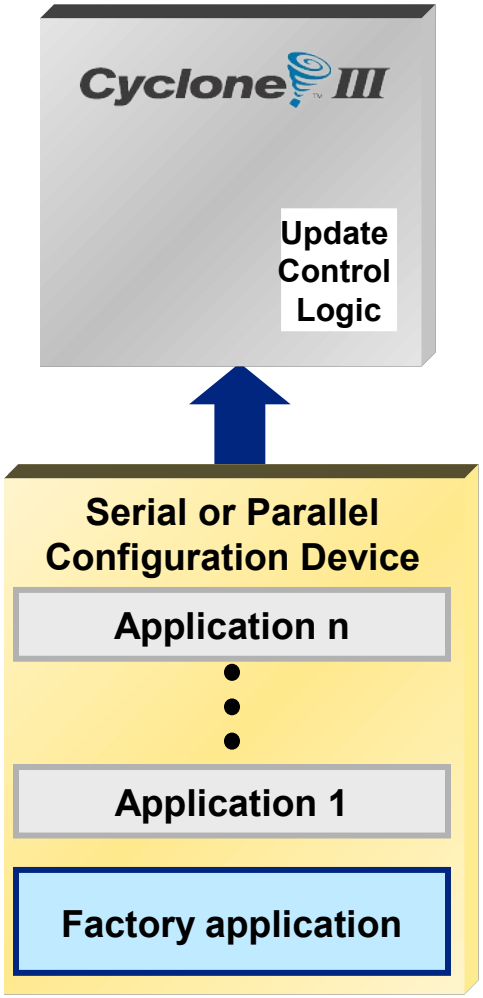
Memory Interfaces That Automatically Calibrate, Track, and Adjust

- Intellectual property (IP) auto calibrates for process differences
  - For both FPGA ***and*** memory
  - Removes timing uncertainties
- Monitors voltage and temperature variations
  - Adjusts resynchronization phase (PLL output)
  - Does not interrupt operation
  - Supports DDR, DDR2, QDR II memories



Increase productivity and minimize timing closure efforts

New Configuration Features



- Multiboot feature allows multiple programming files to be loaded into the FPGA, and protect against remote system upgrade configuration failures
- Remote system update no longer requires external host, saves board space

A Complete Solution

Nios® II

Embedded soft-core processors

Intellectual property

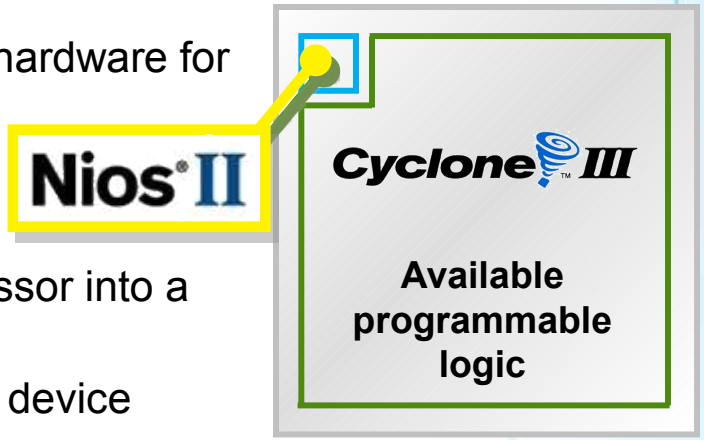
QUARTUS® II

Design software

Development kits

Nios II Embedded Processor

- Choose the *exact* set of CPUs, peripherals, and memory you need for your application
  - Achieve over 160 DMIPs of performance
  - Build custom instructions
  - Accelerate with hardware—C2H compiler automatically converts C subroutines into hardware for Nios II embedded processor
- Low cost
  - Integrate your peripherals and microprocessor into a single chip
  - Support for multiple processors in a single device
  - Implement a processor for $0.25 of logic on a Cyclone III FPGA



Industry's leading soft-core processor

Cyclone III Family Plan

Device	LEs	M9K memory blocks	Total memory (Mbits)	18 X 18 Multipliers	PLLs	Global clocks
EP3C5	5,136	46	0.4	23	2	10
EP3C10	10,320	46	0.4	23	2	10
EP3C16	15,408	56	0.5	56	4	20
EP3C25	24,624	66	0.6	66	4	20
EP3C40	39,600	126	1.1	126	4	20
EP3C55	55,856	260	2.3	156	4	20
EP3C80	81,264	305	2.7	244	4	20
EP3C120	119,088	432	3.9	288	4	20

Notes:
1. Selected product lines are available in commercial, industrial, extended industrial, and automotive temperature variants.
2. Selected product lines/packages offer the following speed grades: -6 (fastest), -7, and -8.

Cyclone III Package Offerings

Device	E144 0.5 mm 22 x 22	M164 0.5 mm 8 x 8	Q240 0.5 mm 35 x 35	F256 1.0 mm 17 x 17	U256 0.8 mm 14 x14	F324 1.0 mm 19 x 19	F484 1.0 mm 23 x 23	U484 0.8 mm 19 x19	F780 1.0 mm 29 x 29
EP3C5	94	106		182	182				
EP3C10	94	106		182	182				
EP3C16	84	92	160	168	168		346	346	
EP3C25	82		148	156	156	215			
EP3C40			128			195	331	331	535
EP3C55							327	327	377
EP3C80							295	295	429
EP3C120							283		531

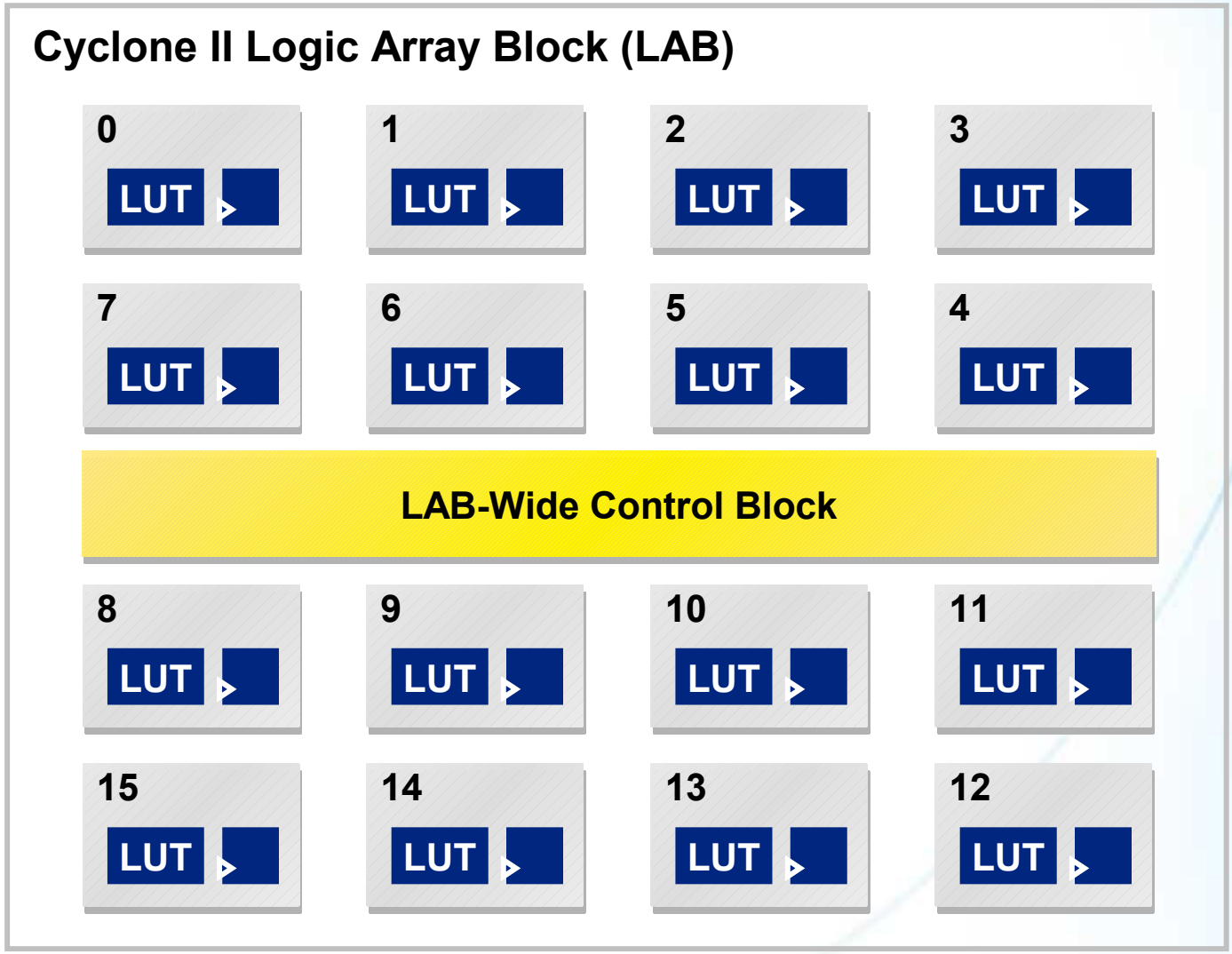
New!

Denotes vertical migration support

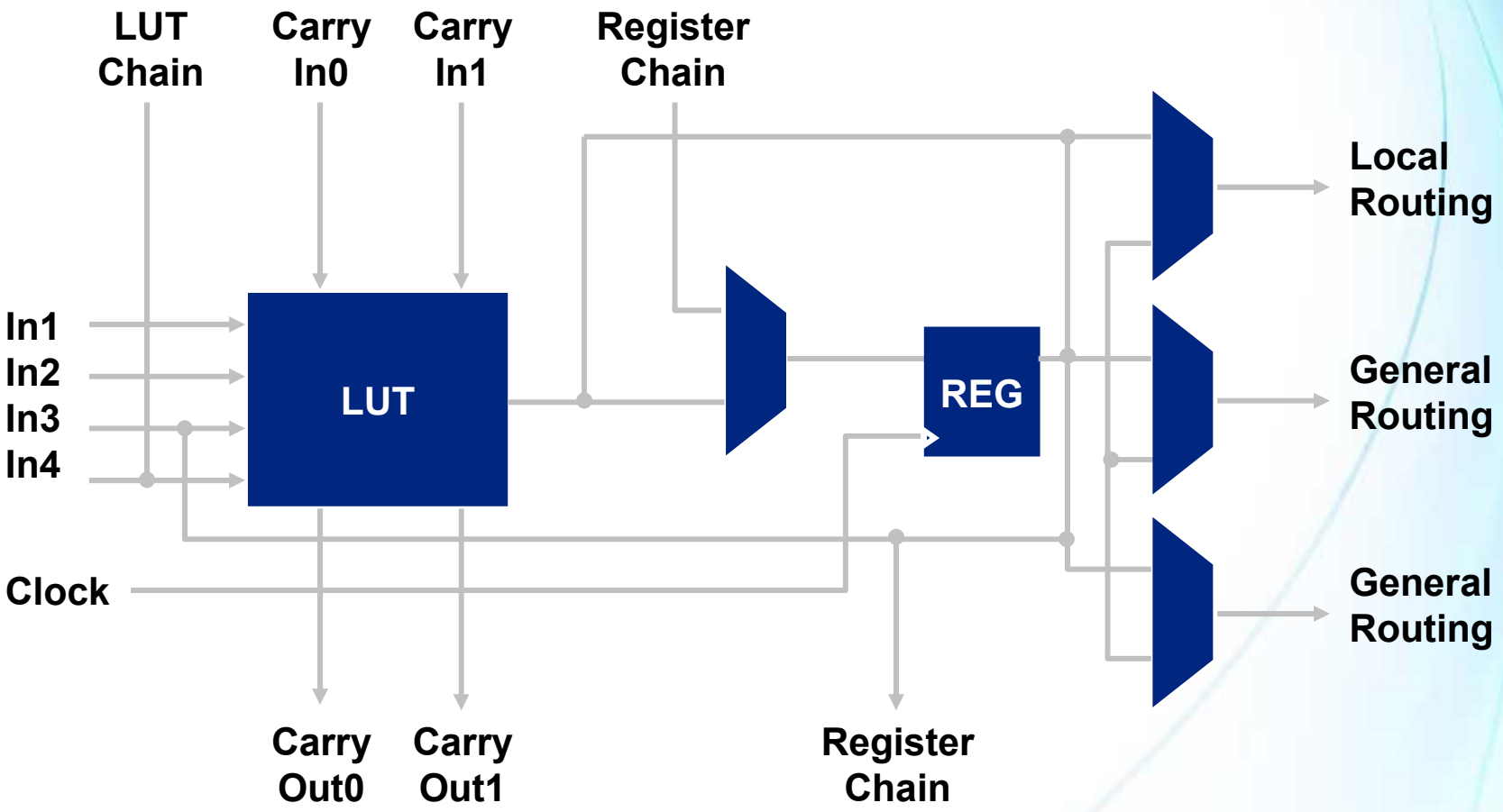
Optimized to offer the highest logic, memory, multiplier, and I/O resources

Technical Details

Cyclone II LAB Structure

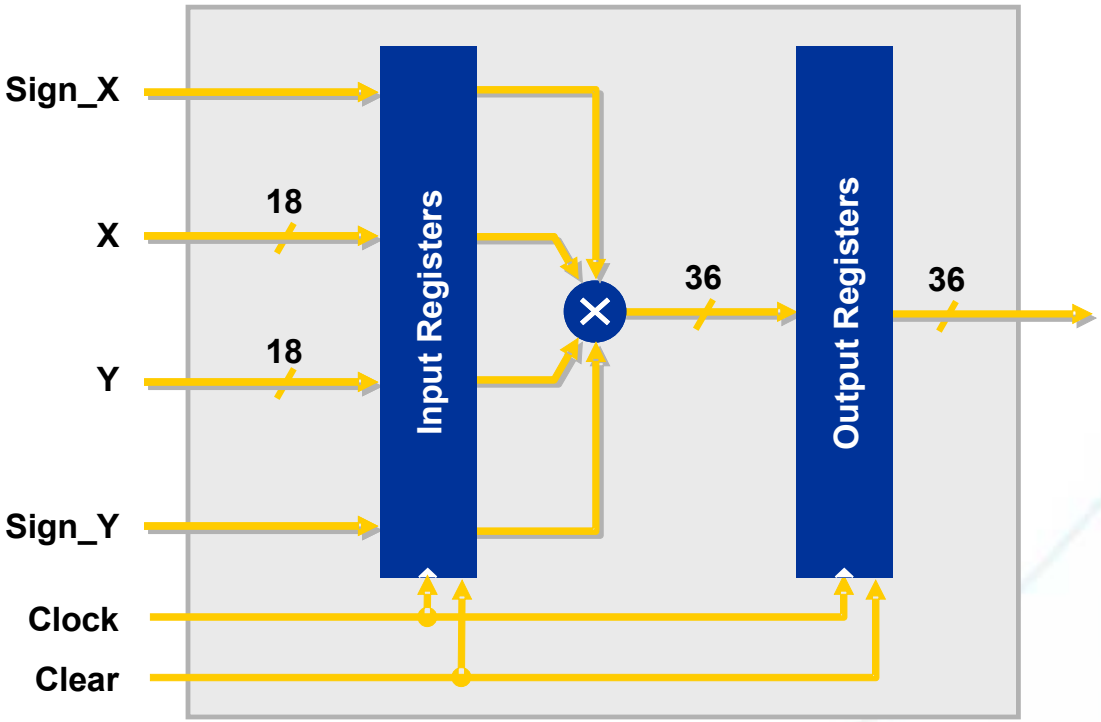


Cyclone II Logic Element



Embedded Multiplier Functionality

- Up to 260-MHz performance
- Supports full-precision 18-bit or 9-bit mode
  - One 18-bit or two 9-bit multipliers per block



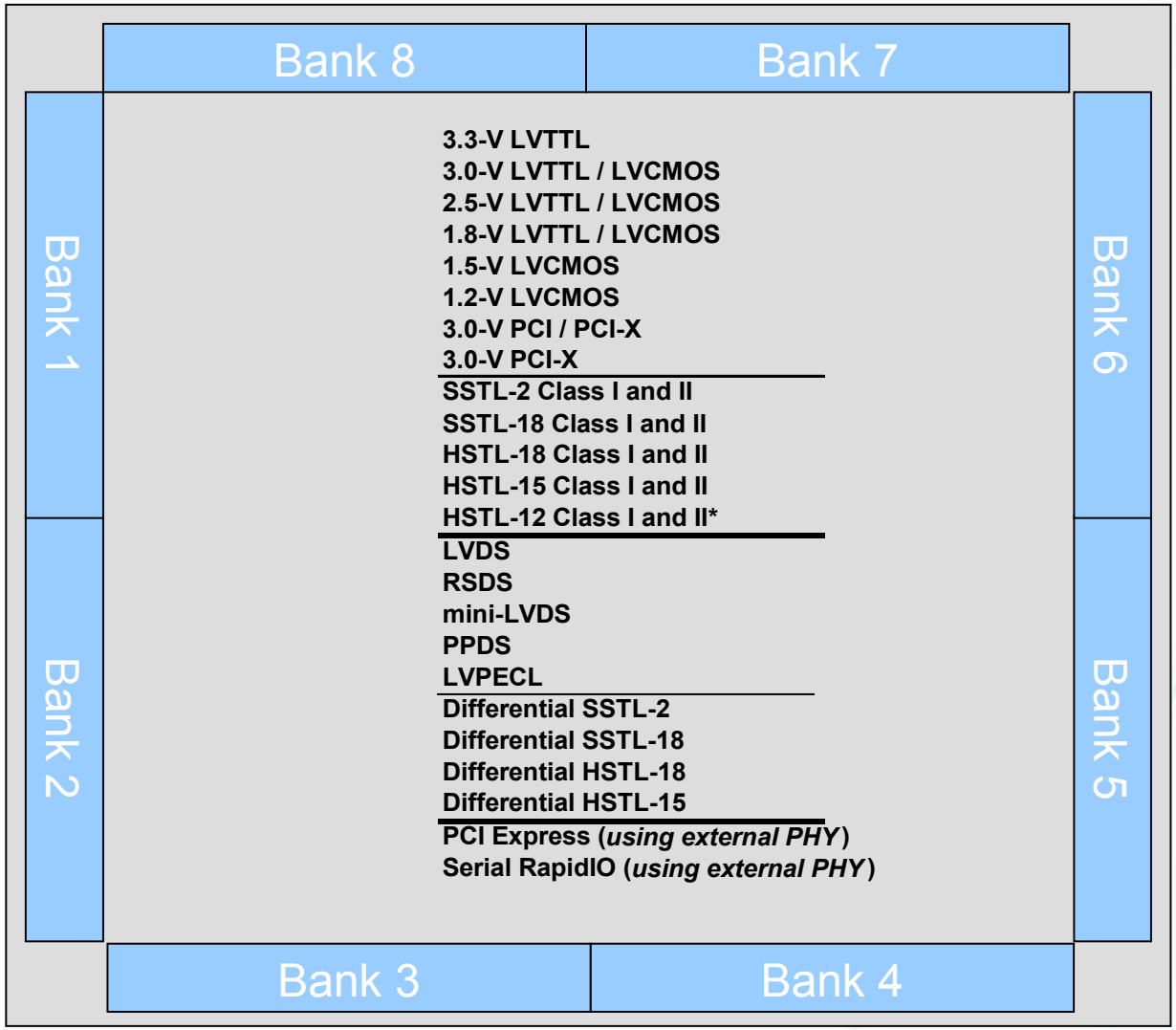
On-Chip Memory Enhancements

Feature	Cyclone II (M4K)	Cyclone III (M9K)	Benefit
Block Size	4 Kbits	9 Kbits	Increased Memory
Performance	216 MHz	260 MHz	Faster Performance
Dual-Port Read During Write Behavior	New Data ("Flow Thru")	New Data or Old Data	Flexibility and Ease of Use
Parity Bit	Yes	Yes	Usability for High Reliability Apps
Clock Enables	2	4	Increased Flexibility and Reduced Power
Read and Write Enables	2	4	Increased Flexibility and Reduced Power

I/O Enhancements

I/O Enhancement	Benefit
All Interfaces and Standards Supported on all Banks	**-Allows flexible I/O placement for easier PCB design reduced board area**
Enhanced LVDS Buffers	-Eliminates external resistors for LVDS, RSDS, and mini-LVDS transmission -Increases LVDS interface performance – up to 875 Mbps (Rx) & 840 Mbps (Tx)
Selectable Series OCT with Calibration	-OCT Eliminates external resistors -Improves signal integrity and performance with selectable impedance matching -Calibration eliminates variations due to PVT
Two Additional I/O Element Registers	-Increases external interface performance -Improves Tco performance
Adjustable Slew Rates	-Improves signal integrity by slowing down edge rates on non-performance critical I/O pins

All I/O Standards On All Banks



*HSTL-12 Class II is only supported on top and bottom banks

Supported I/O Standards

Single-Ended I/O Standards	Max	Usage
2.5-V SSTL Class I and II	167 MHz	DDR SDRAM
1.8-V SSTL Class I and II	200 MHz	DDR/DDR2 SDRAM
1.8-V/1.5V/1.2-V HSTL I and II	167 MHz	QDR II SRAM
3.3-V PCI Compatible	66 MHz	Embedded
3.3-V PCI-X 1.0 Compatible	100 MHz	Embedded
3.3-V LVTTL	**100 MHz***	System Interface
3.0-V/2.5-V/1.8-V LVTTL	167 MHz	System Interface
3.0-V*/2.5-V/1.8-V/1.5-V/1.2-V LVCMOS	167 MHz	System Interface

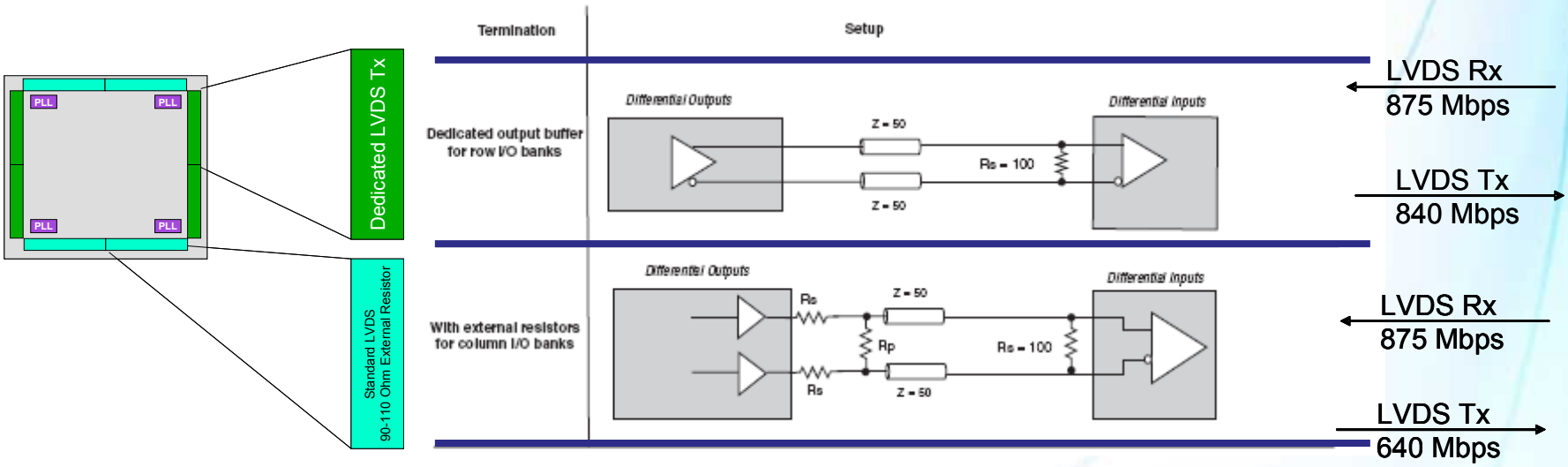
Differential I/O Standards	Max	Comment
LVDS	875 Mbps	High-Speed Serial
RSDS/Mini-LVDS Transmission	440 Mbps	High-Speed Serial
LVPECL	500 MHz	High-Speed Clocks
PCI Express*	2.5 Gbps	Per Channel
Serial RapidIO*	3.125 Gbps	Per Channel

*Different from BA presentation

*IP cores available, requires external PHY devices

Enhanced LVDS Buffers

- Dedicated LVDS Output Buffers on the left and right banks
  - Increased performance, 840 Mbps
  - No external resistors required
- Improved LVDS Input Buffers on all banks
  - Increased performance, 875 Mbps



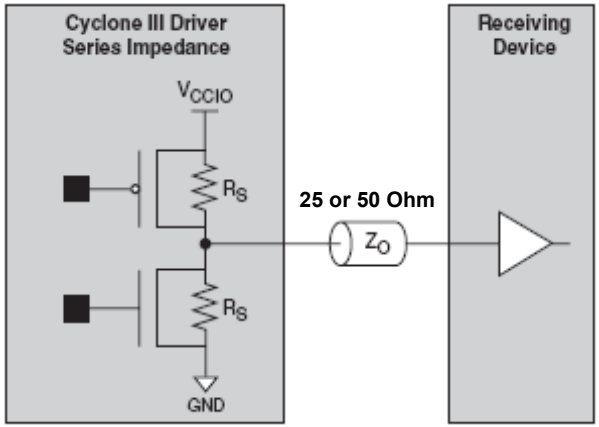
LVDS Pairs Reference

Package	Device	Total I/O	LVDS Pairs		
			With Dedicated Output Buffers	Without Dedicated Output Buffers	Total
E144	3C10	85	5	7	12
	3C16	67	3	4	7
	3C25	65	4	2	6
Q240	3C16	143	17	18	35
	3C25	131	17	14	31
	3C40	111	7	7	14
F256	3C10	173	21	36	57
	3C16	151	19	24	43
	3C25	139	18	24	42
F324	3C25	198	29	42	71
	3C40	178	22	27	49
F484	3C16	329	66	62	128
	3C40	314	58	56	114
	3C55	310	61	62	123
	3C80	278	53	48	101
F780	3C40	518	110	105	215
	3C55	360	68	83	151
	3C80	412	77	92	169

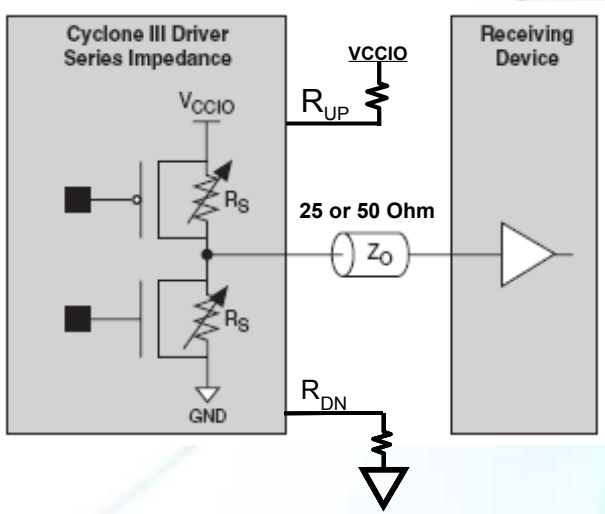
OCT With Calibration

- Output buffer impedance may vary slightly due to PVT
- With OCT Calibration, after configuration the output buffer impedance is automatically adjusted to match two external resisters (RUP & RDN), which are either 50 Ohms or 25 Ohms

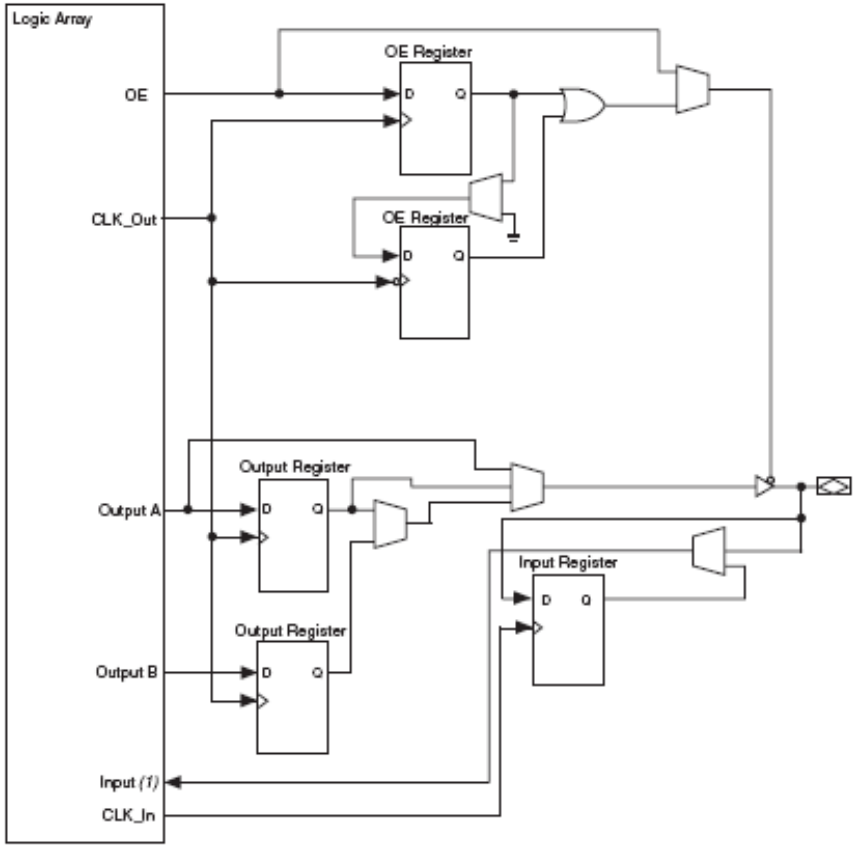
OCT Without Calibration



OCT With Calibration



Two additional I/O element registers



Memory	Cyclone II Performance	Cyclone III Performance	Increase
DDR2	167 MHz	200 MHz	20%

Improved Memory Performance and Flexibility

Slew Rate Control

- Available for all single ended I/O standards, with drive strengths of 8 mA or more (*except 3.3-V LVTTL*)
- Selectable on a pin by pin basis, using the Quartus II Software assignment editor
- Three settings: fast, medium, slow
- Default is fast

Cyclone III – The Right Balance

- The benefits of leading edge technology
  - 300 mm wafers
  - TSMC's 65 nm low power process
- With 3.3-V I/O support
  - 3.3-V I/O driven from 3.3-V VCCIO, or
  - 3.3-V I/O driven from 3.0-V VCCIO
- As long as a few simple guidelines are followed
  - See AN 447

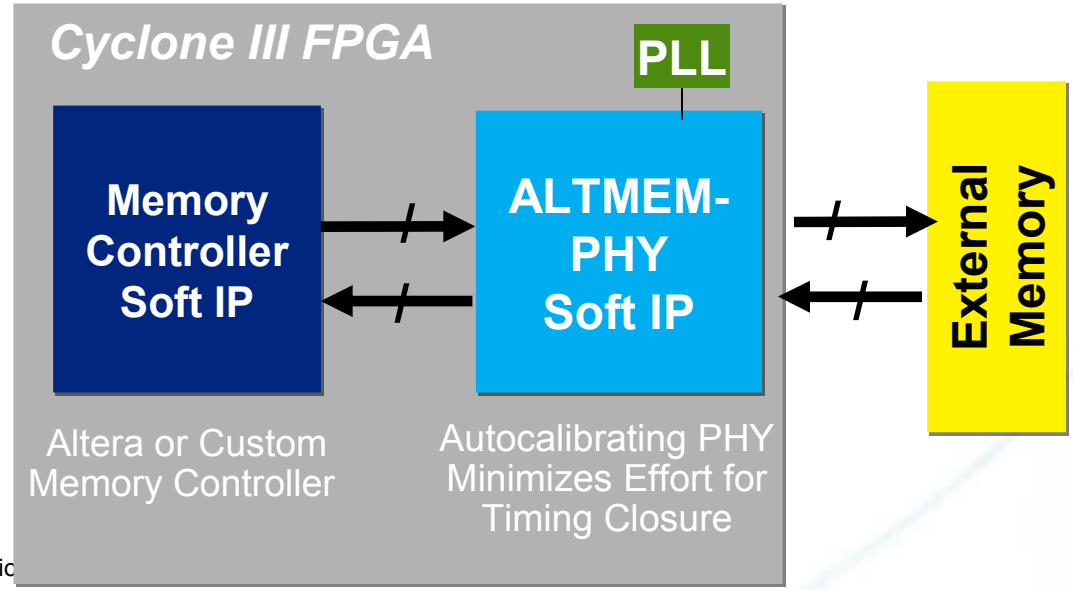
Cyclone III External Memory Support

Memory Standards	C6 (MHz)		C7 (MHz)		C8 (MHz)		Availability
	Col I/O	Row I/O	Col I/O	Row I/O	Col I/O	Row I/O	Quartus II software version
DDR1 SDRAM	167	150	150	133	133	125	6.1
DDR2 SDRAM	200	167	**167**	**150**	150	133	6.1
QDRII SRAM	167	150	150	133	133	125	Q2 '06

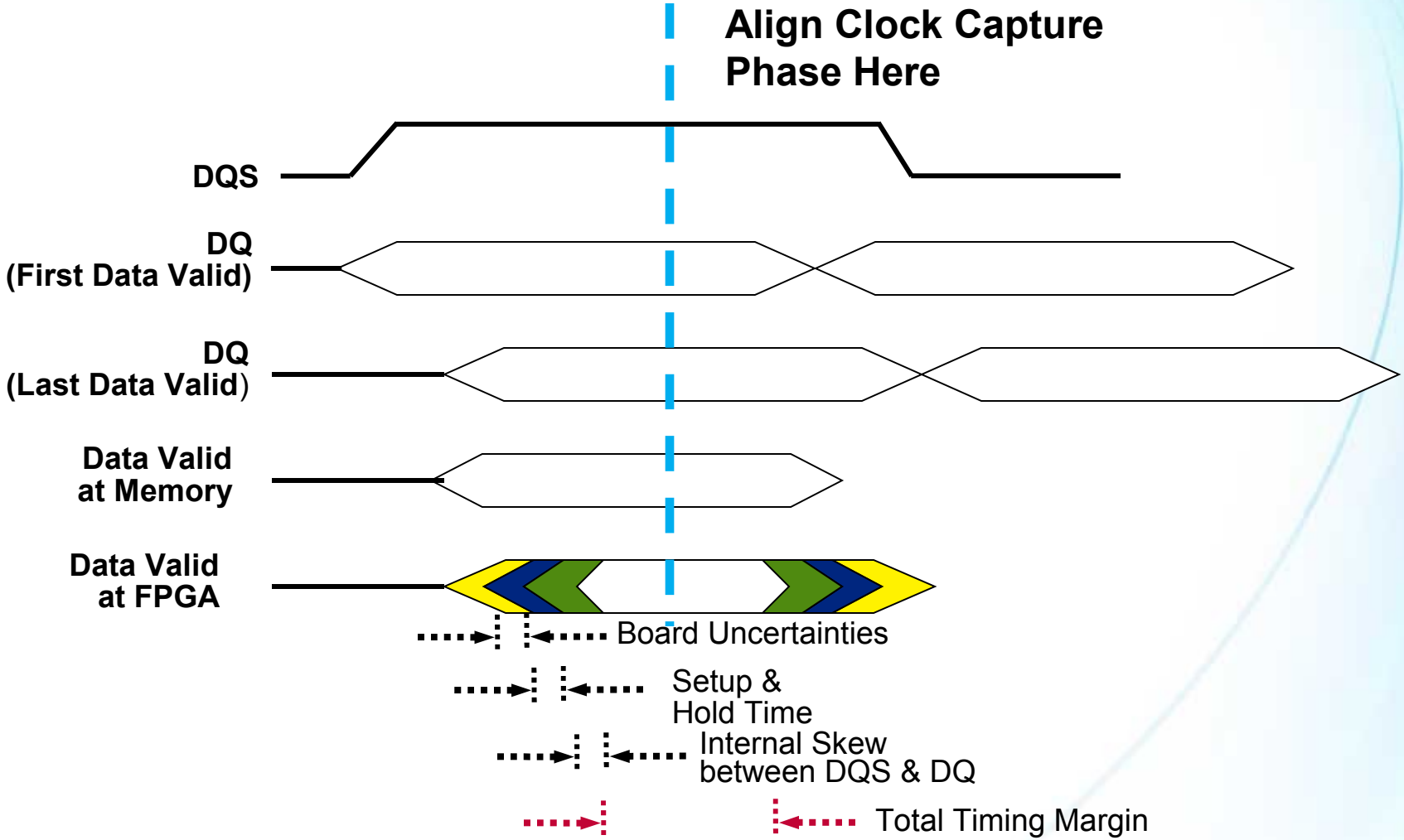
- All numbers are minimum frequencies achievable; maximum frequencies pending characterization

ALTMEMPHY Physical Interface

- Soft megafunction included with all versions of the Quartus II software
- Self-calibrating at startup:
  - FPGA and memory device process changes
  - System uncertainties
- Periodic calibration during operation
  - Voltage and temperature changes
- Push button timing closure
- Better performance for fast and slow speed grade devices

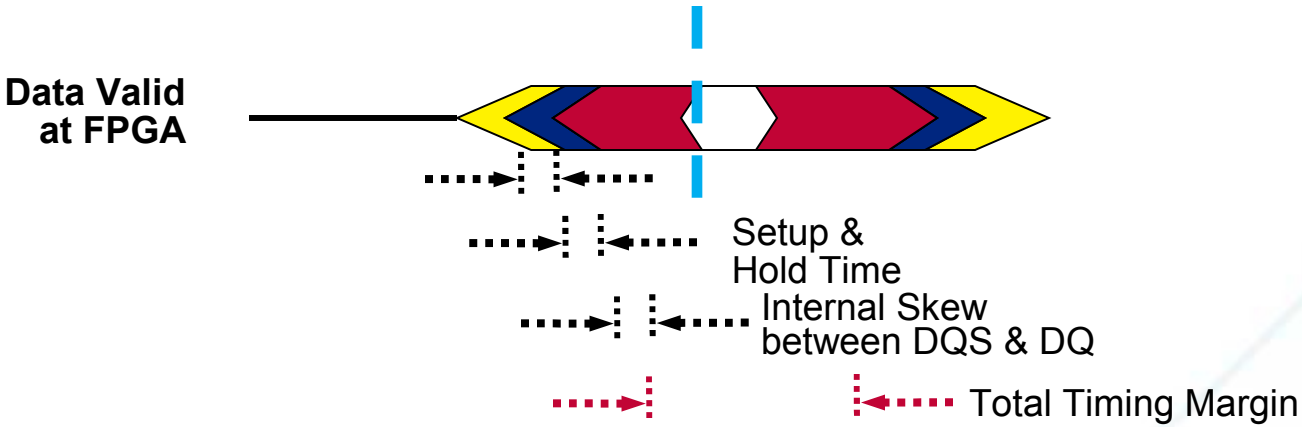


Timing Margins Are Shrinking



Additional Uncertainties

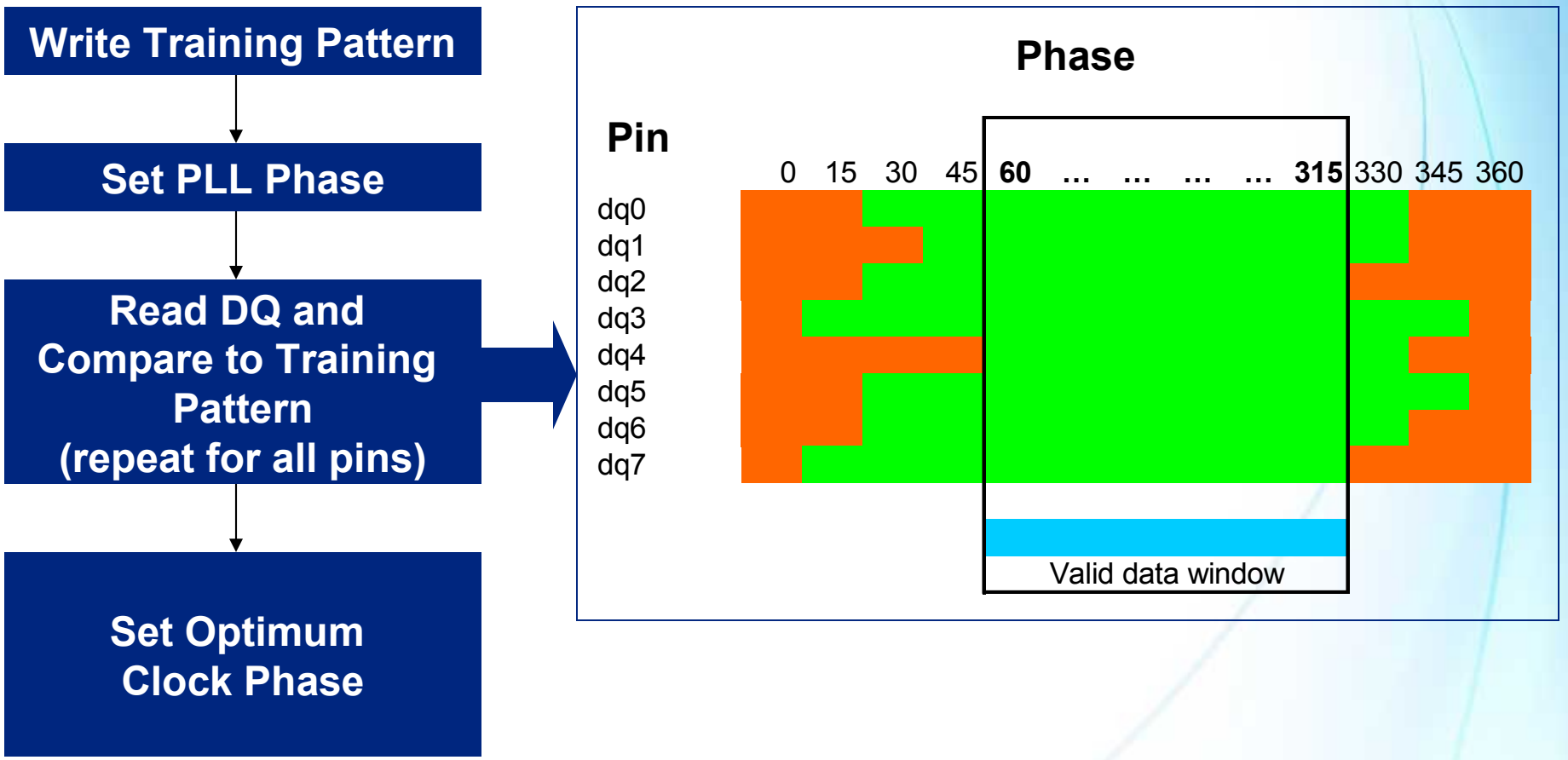
- Temperature and voltage changes
- Process variations over time
- Memory vendor changes
- Board layout changes



PLL Dynamic Phase Adjustment

- Dynamic adjustment of PLL phase setting
- Increase/decrease 1 step at a time
  - Step increments depend on PLL configuration

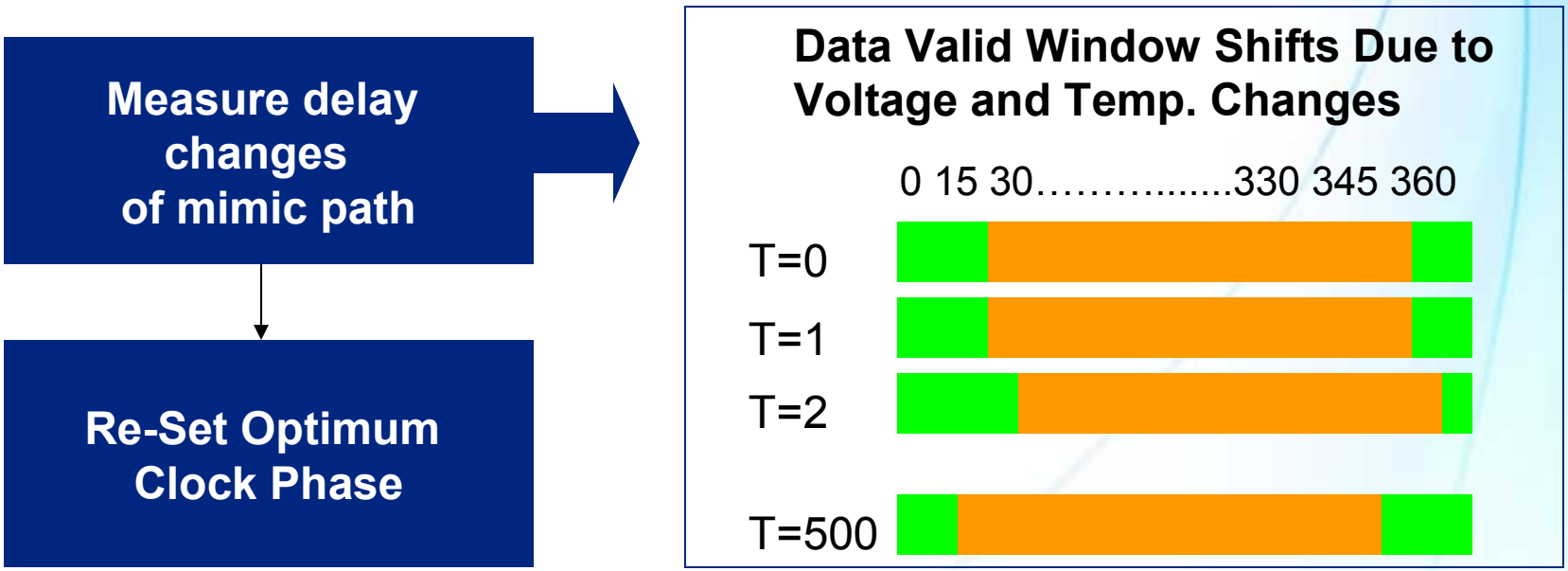
Calibration at Startup



PHY adapts to your system!

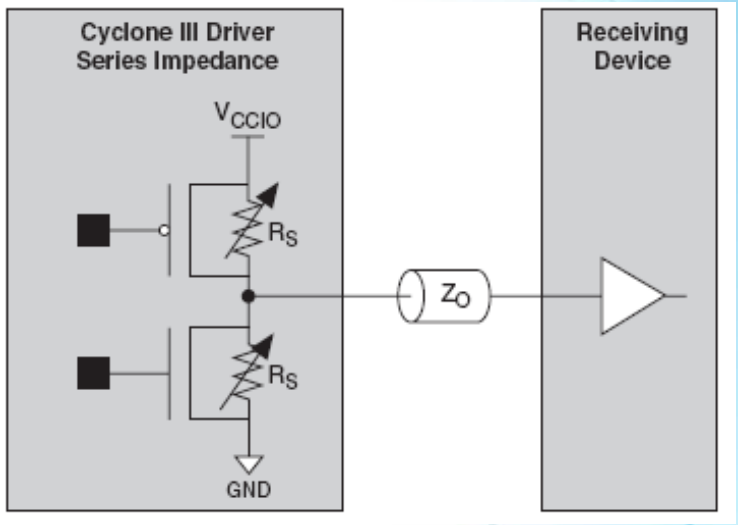
Periodic Calibration

- Data capture and measurement of a representative mimic path delay every 128 ms
  - Path delay may change due to voltage and temperature changes
  - Assumption: Data Valid window drift due to temperature and voltage similar to delay change of representative path
- Non-Intrusive dynamic phase adjustment



Signal Integrity

- Series On-Chip Termination
  - Match output driver impedance to trace impedance
  - Calibrated on power up for process, temperature, and voltage variations
- Adjustable Slew Rates
  - Choose slower slew rates to lower simultaneously switching output (SSO) effects
- IBIS models for board simulation
  - Pending characterization



Flexible PCB Layout

- Interfaces available on all sides

Table 4. Cyclone III DQS and DQ Bus Mode Support for Each Side of Device (1) (Part 3 of 4)

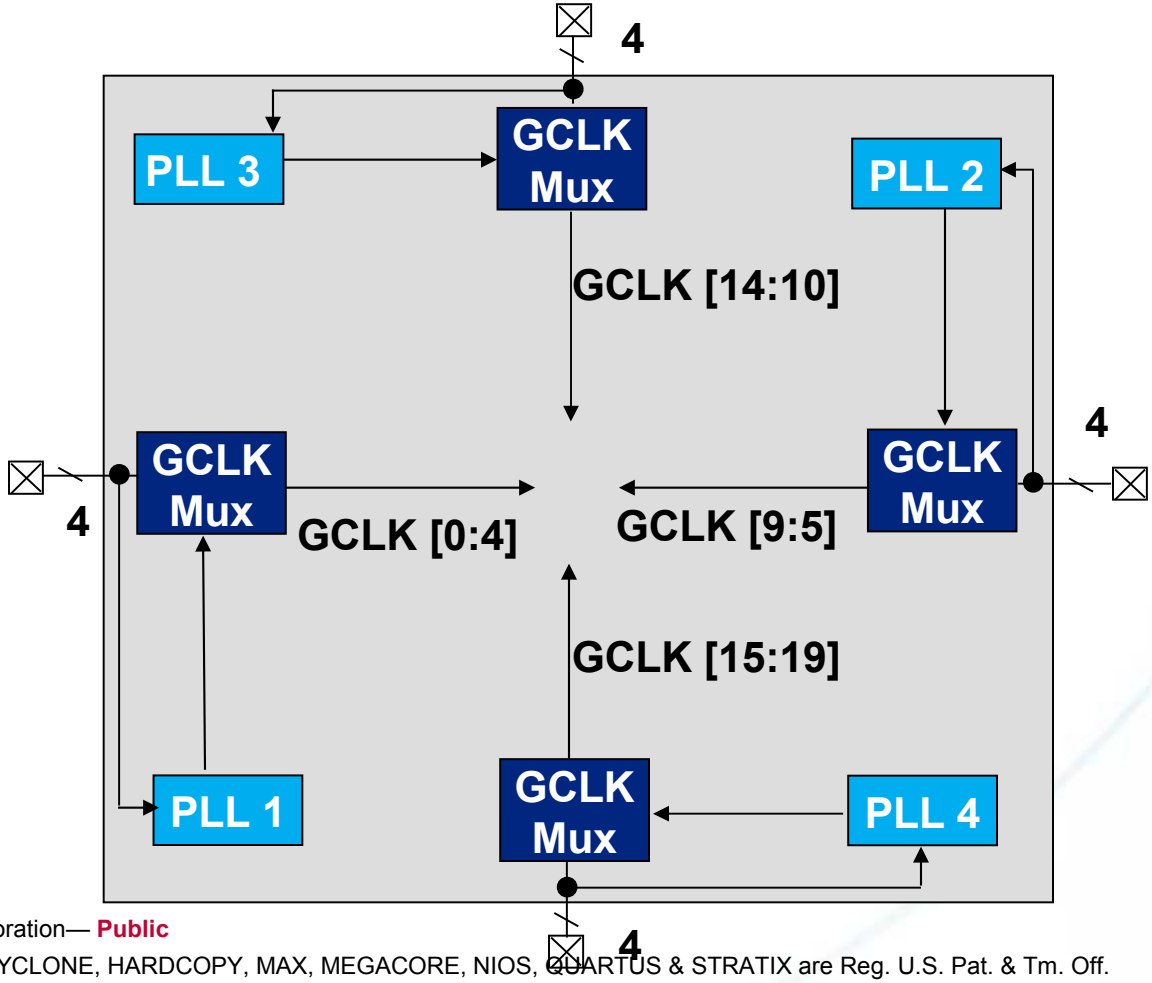
Device	Package	Side	Number of ×8 Groups	Number of ×9 Groups	Number of ×16 Groups	Number of ×18 Groups	Number of ×32 Groups	Number of ×36 Groups
EP3C40	484-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1

Clock Networks & PLLs Overview

- Flexible clock management resources maximize system integration capabilities
  - PLL features
    - Dynamic phase adjustments enable self-calibrating external memory controllers
    - Reconfiguration enables display applications where the input frequency is unknown
    - Generate up to 10 internal clocks and 2 external clocks from a single clock source
    - 5 outputs per PLL combined with new IP enables x72 DDR2 interfaces using just 1 PLL
  - Unused clock networks are turned off to minimize power consumption
  - Global clock networks double as low skew, high fanout control signals

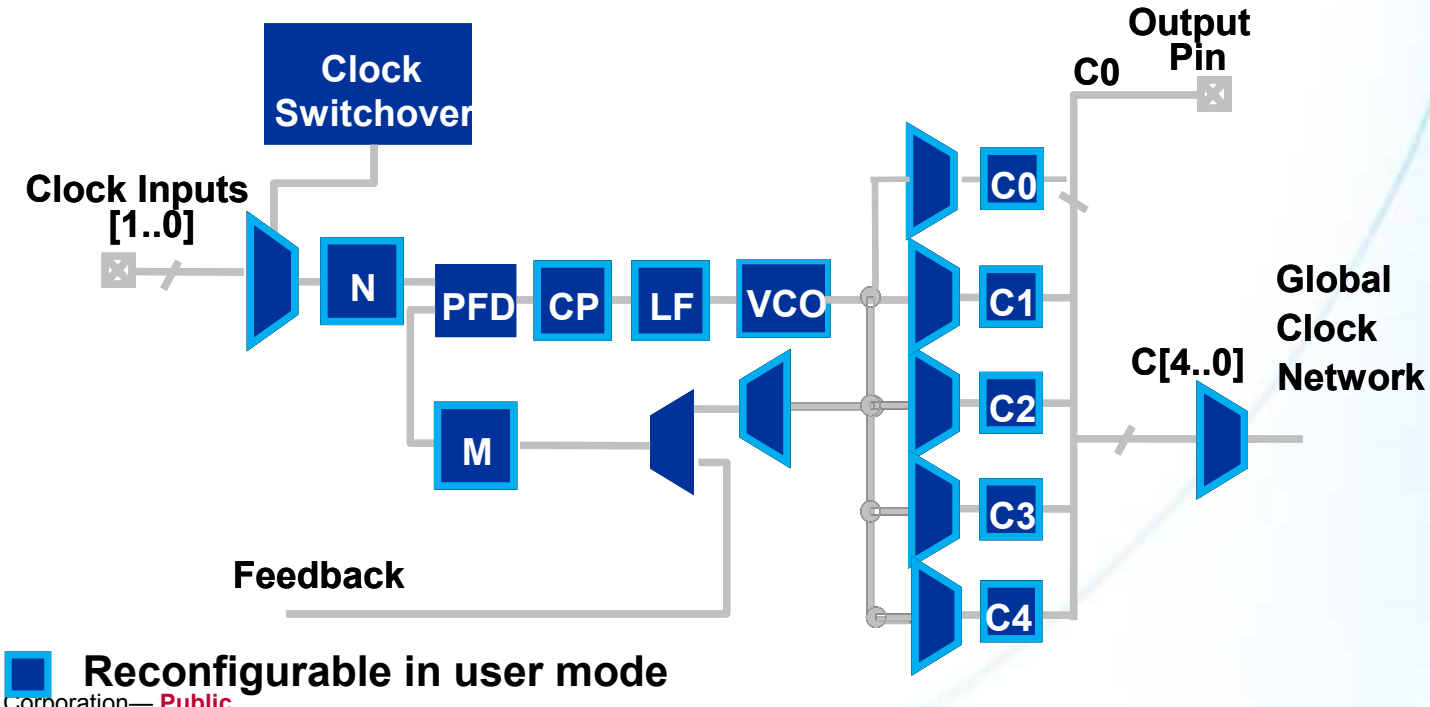
Clock Networks & PLLs Overview

- Up to 20 Global Clocks Per Device
- Dual purpose as high fan out control signals

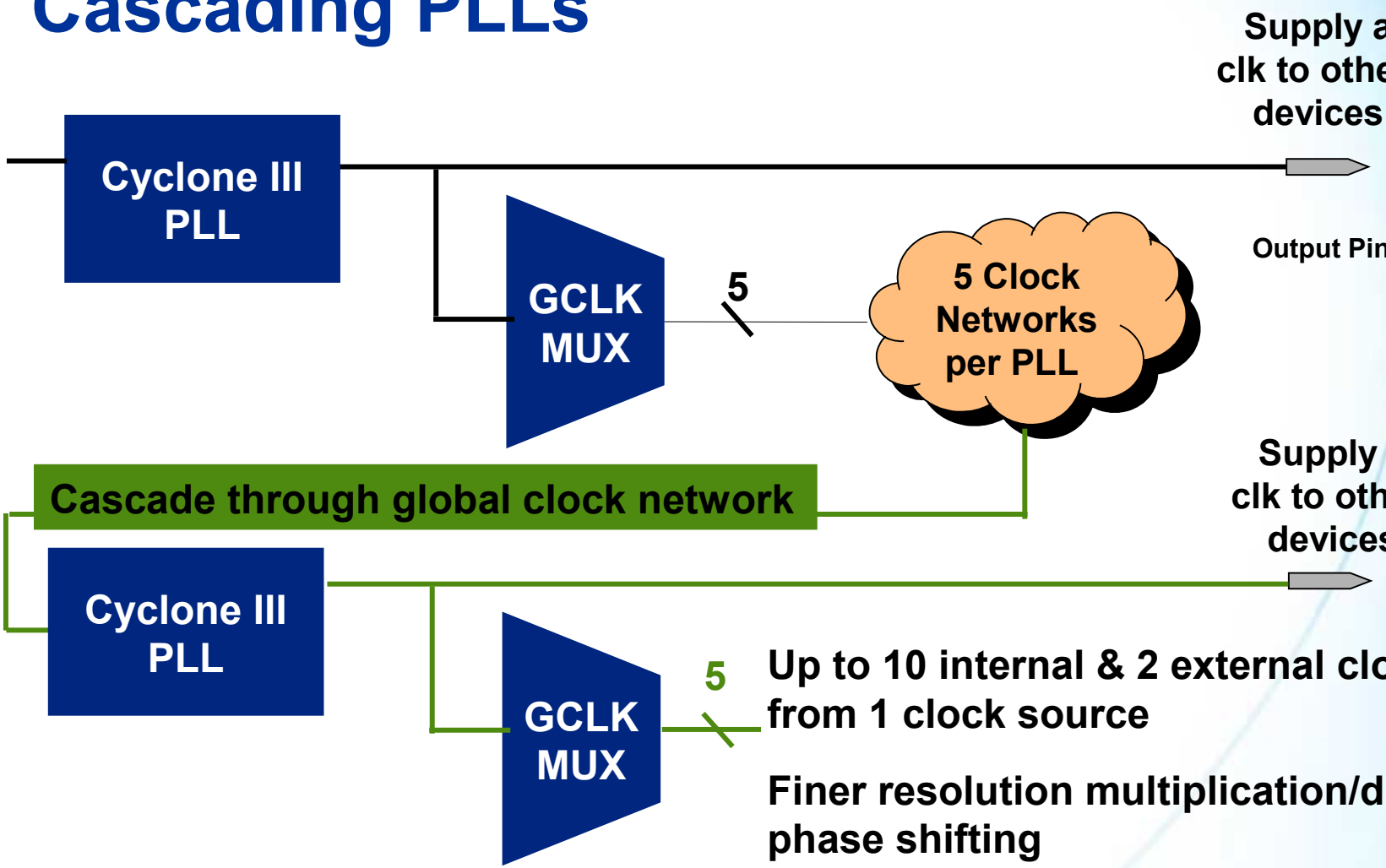


Cyclone III PLL Functions

- Clock Multiplication & Division
- Clock Synthesis
- Phase Alignment & Phase Shift



Cascading PLLs



Up to 10 internal & 2 external clocks from 1 clock source

Finer resolution multiplication/division & phase shifting

Clean up low performance and noisy external clock sources

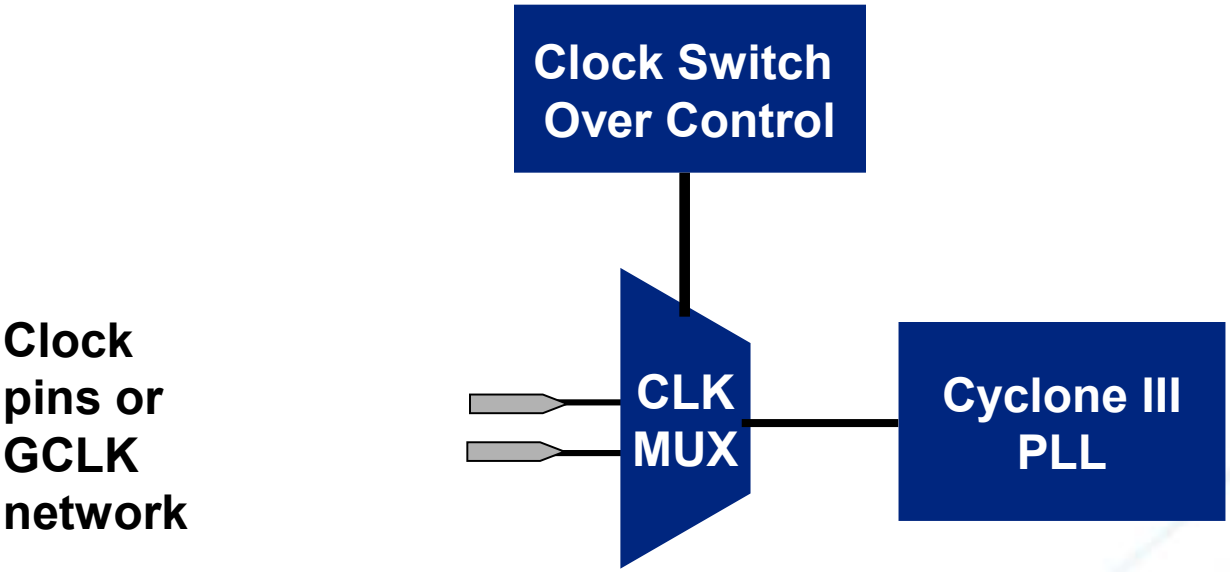
PLL Dynamic Phase Adjustment

- Dynamic adjustment of PLL phase setting
- Increase/decrease 1 step at a time
  - Step increments depend on PLL configuration

Enables Auto-Calibrating PHY for External Memory Interfaces

Clock Switch Over

- Automatically switch from 1 clock to another in the event a clock stops
- Manually switch from 1 clock source to another



Compensation Modes

PLL Mode	Description
Source Synchronous	Clock-to-data relationship at input pin (setup/hold) maintained at the IOE register
No Compensation	No compensation for best jitter performance
Normal	Input clock delay fully compensated for alignment with clock at IOE or core register
Zero Delay Buffer	Input clock aligned with dedicated external clock output

PLL Feature Comparison

	Cyclone II	Cyclone III	Cyclone III Advantages
Number of PLLs	2 – 4	2 – 4	Same
Outputs per PLL	3	5	Up to 8 additional global clocks driven by PLLs
Number of Global Clocks	8 – 16	10 – 20	Combine required clock signals into fewer PLLs
Min, Max Frequency (MHz)	10 – 400	5 – 440	Broader range improves system flexibility
Dynamic Reconfiguration	No	Frequency and Phase	Improve system performance by removing device downtime
Cascadable	No	Yes	Increase PCB routing flexibility

Cyclone III Configuration Overview

- Comprehensive configuration and remote system upgrade solution
  - Simple, easy to use, & low cost
  - Available with option does not require external host
  - Altera serial configuration devices available for all densities
- Commodity Flash configuration
  - Free configuration solution if extra memory is available in a parallel Flash already on board
- Cyclone III serial & parallel Flash loader
  - In system programming of serial and parallel configuration devices through Cyclone III JTAG port

What's New in Cyclone III Configuration?

Active Parallel	– Configuration with commodity parallel Flash already on board without a separate controller – First time for any Altera FPGA
Remote System Upgrade	– No external host required – Available with Active Serial or Active Parallel configuration mode
Fast-On	– Option to reduce maximum POR time to 9ms to meet automotive 100 ms "wake up" time requirements
Fast Passive Parallel	– Fastest configuration option – Allows 100 MHz clock with x8 data width

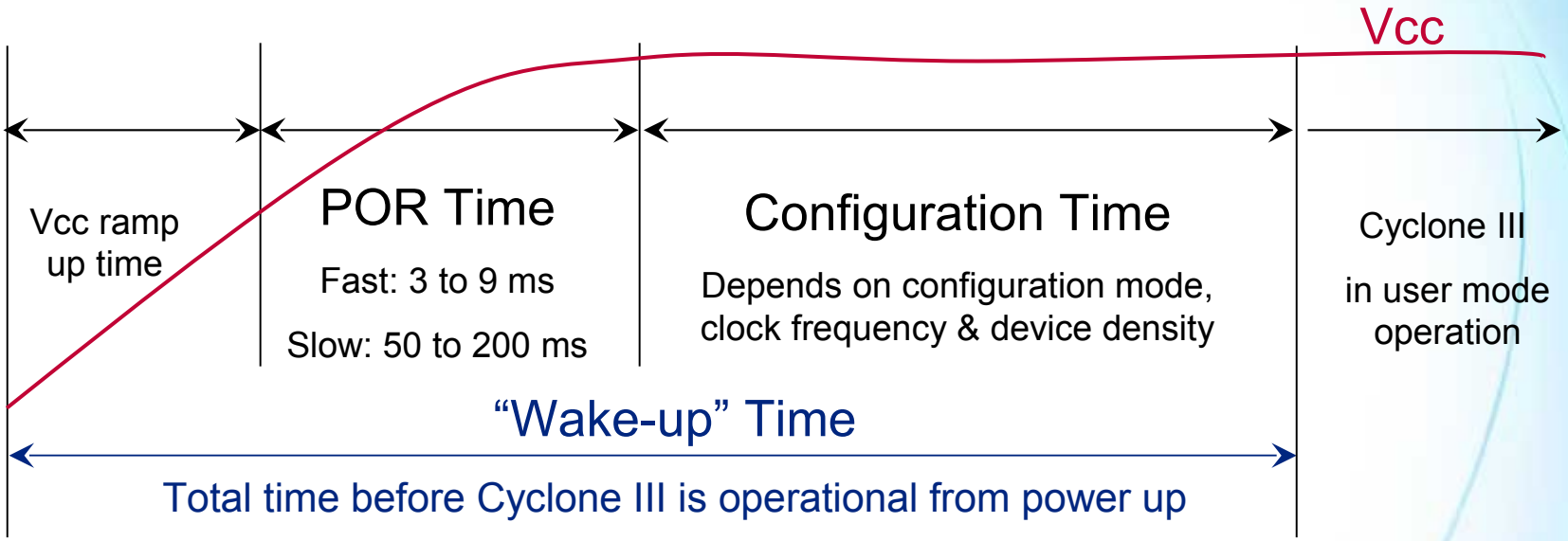
Configuration Mode Overview

Programming Mode	*Cyclone III*	*Cyclone I & II*	*Stratix III*	*Stratix II*	*Stratix*
Active Serial	✓	✓	✓	✓	
Active Parallel	✓				
Passive Serial	✓	✓	✓	✓	✓
Fast Passive Parallel	✓		✓	✓	✓
JTAG	✓	✓	✓	✓	✓
Remote Update	✓		✓	✓	✓

First time for Cyclone Family FPGAs

- Active: Controller in FPGA & Clock is from FPGA
- Passive: Controller outside of FPGA & Clock is supplied from outside controller

Understanding Configuration Timing



- Application with fast "Wake-up" time specification needs to utilize fast POR time and fast configuration modes
- POR time and configuration time user configurable with mode select pins(MSEL3..0)
- Fast POR option requires fast* Vcc ramp

* Vcc ramp time needs to be faster than POR Time. Specification will be determined after characterization

** Only major timings are shown above

Configuration Mode Comparison

Configuration Mode	*Ease of Use[a]*	*Config Speed[b]*	*Additional # Chips Required*	*# of Cyclone III Pins[c]*	*Data Compre-ssion*	*Remote Upgrade*
Active Serial	**1**	**292ms**	**1**	**4**	✓	✓
Active Parallel	**2**	**48ms**	**1**	**47**		✓
Passive Serial	**3**	**117ms**	**2**	**2**	✓	
Fast Passive Parallel	**4**	**38ms**	**2**	**9**		
JTAG[d]	**5**	**210ms**	**2**	**4**		

a. Ease of Use: Subjective rating based on number of chips, number of I/Os required, and additional knowledge requirement (1 being the easiest solution)

b. Benchmark based on 3C80 at maximum frequency for each mode

c. Pin count excluding MSEL3..0, nStatus, CONF_Done, nCE, and nCEO

d. JTAG using an external controller and a Flash device

Configuration File Size & Time

Device	File Size* (Mbits)	Compressed Size (Mbits)	AS** (ms)	AP (ms)	FPP (ms)
EP3C5	3.3	1.9	49	5	4
EP3C10	3.3	1.9	49	5	4
EP3C16	4.3	2.4	63	7	6
EP3C25	6.2	3.4	90	10	8
EP3C40	10.0	5.6	146	16	13
EP3C55	15.3	8.5	222	25	20
EP3C80	20.0	11.1	292	33	26
EP3C120	29.1	16.2	424	48	38

Clock Frequency for Active Serial (AS): 40Mhz***, Active Parallel (AP): 40Mhz***, Fast Passive Parallel (FPP): 100Mhz

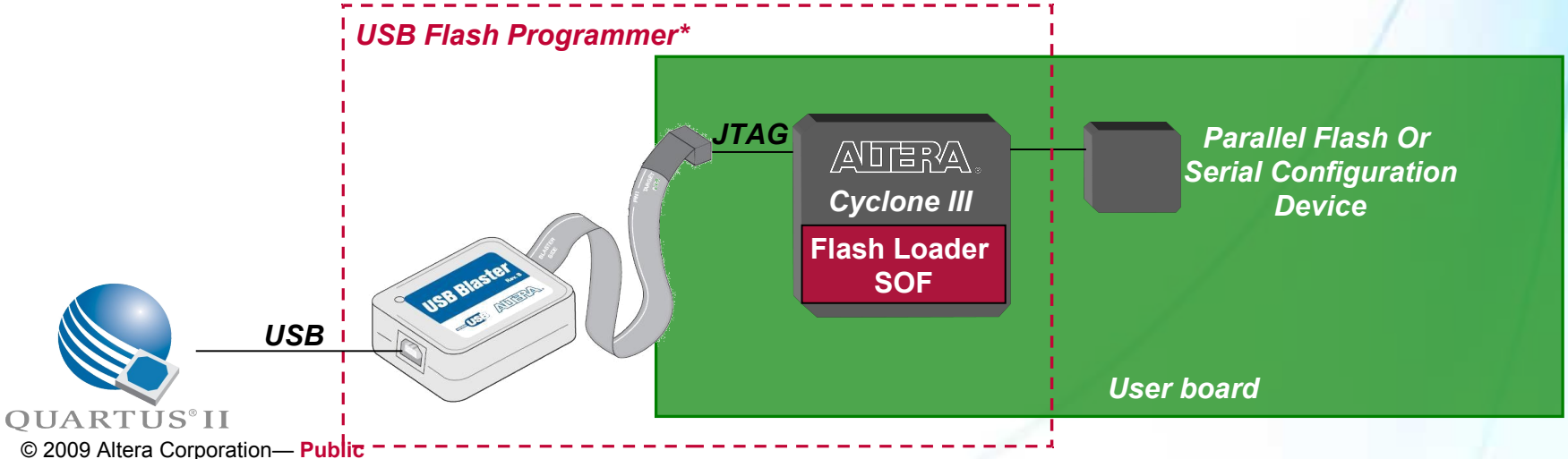
* Preliminary information

** Configuration Time using compressed data for AS mode

*** Max/Typ/Min = 40Mhz/30Mhz/20Mhz, configuration times can be up to 2X longer than values in table for AS and AP modes

Programming Flash in System

- Program or examine Flash device from Quartus II programmer window
  - Cyclone III works as a Flash programmer with Flash loader SOF
  - Quartus II downloads SOF automatically & programs Flash
- Eliminates additional hardware and software for on board Flash programming
  - Unique tool for Altera



* ByteBlaster & EthernetBlaster works identically

Cyclone III Remote System Upgrade

- Allows multiple new application images in addition to factory image
- Built in recovery circuitry loads factory image if upgrade image fails to load
- No external host or processor required
- Customize with Nios II or user-defined control logic

Remote System Upgrade

- Utilize in application where time to market is critical
  - Ship initial product with minimum feature set
  - Remotely upgrade system without system being down due to upgrade failure
  - Can be used for bug fix and/or upgrade application