



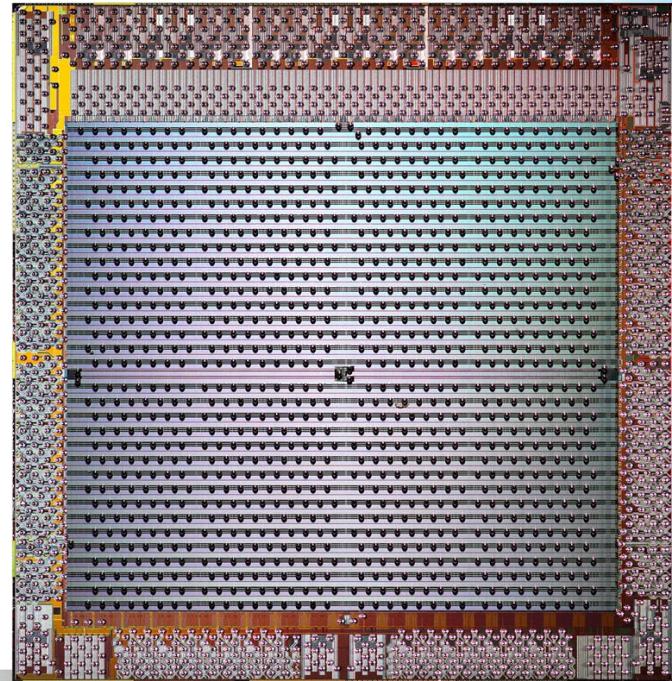
## Arria II GX Family

*The Only Low-Cost FPGAs with  
High-End Capabilities*



# Presentation Contents

- Introduction
- Architecture overview
- Advanced FPGA fabric
- Transceiver technology and protocol support
- Internal memory resources
- DSP resources
- External memory interfaces
- Single-ended I/Os
- LVDS
- Design security
- Design development resources
- PCIe in 45 minutes
- Family plan
- Package plan



***Now Shipping!***

# Arria II GX FPGA: Low Cost for High-End Capabilities

## ■ Low cost

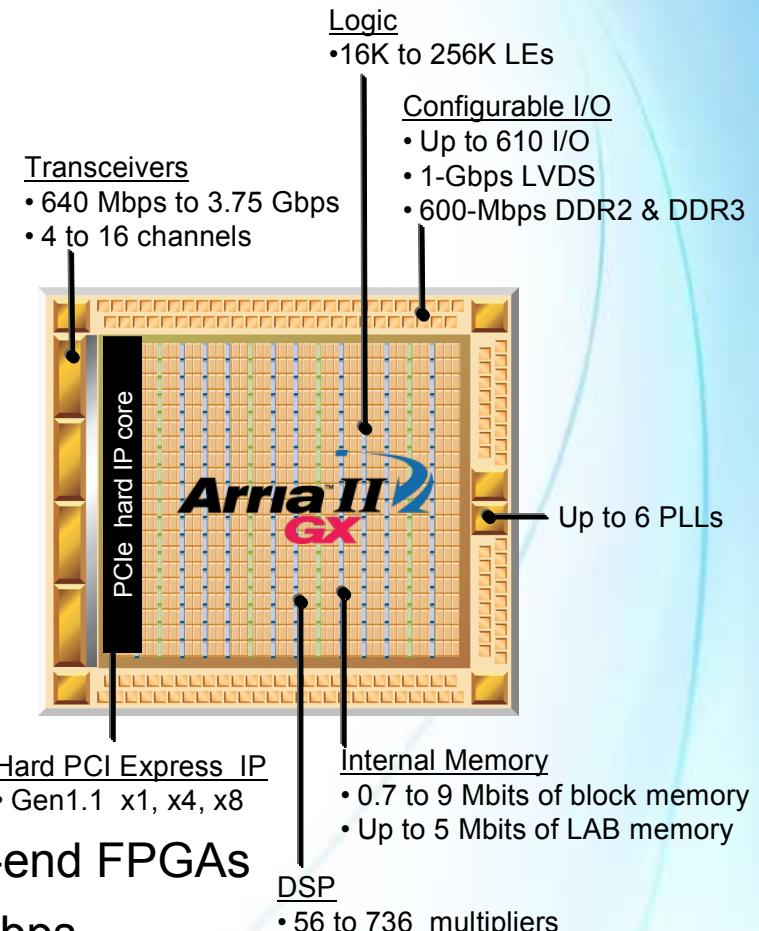
- Half the price of competing high-end FPGAs

## ■ High functionality

- High-performance ALM-based fabric
- High density - up to 260K LEs
- Up to 16 transceivers @ 3.75 Gbps
- Up to 12 Mbits of memory
- Highest ratio of DSP-to-logic resources

## ■ Low power

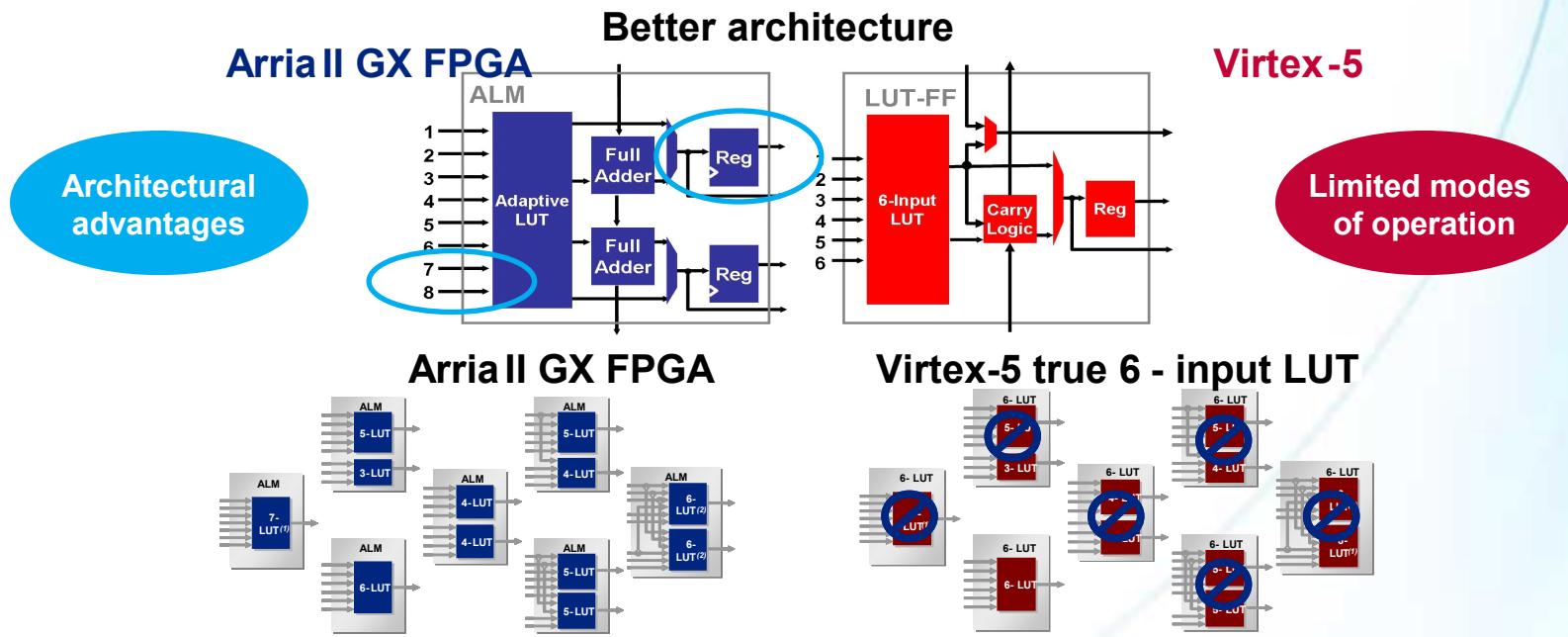
- Up to 50% lower power than competing high-end FPGAs
- <100mW per transceiver channel @ 3.125 Gbps



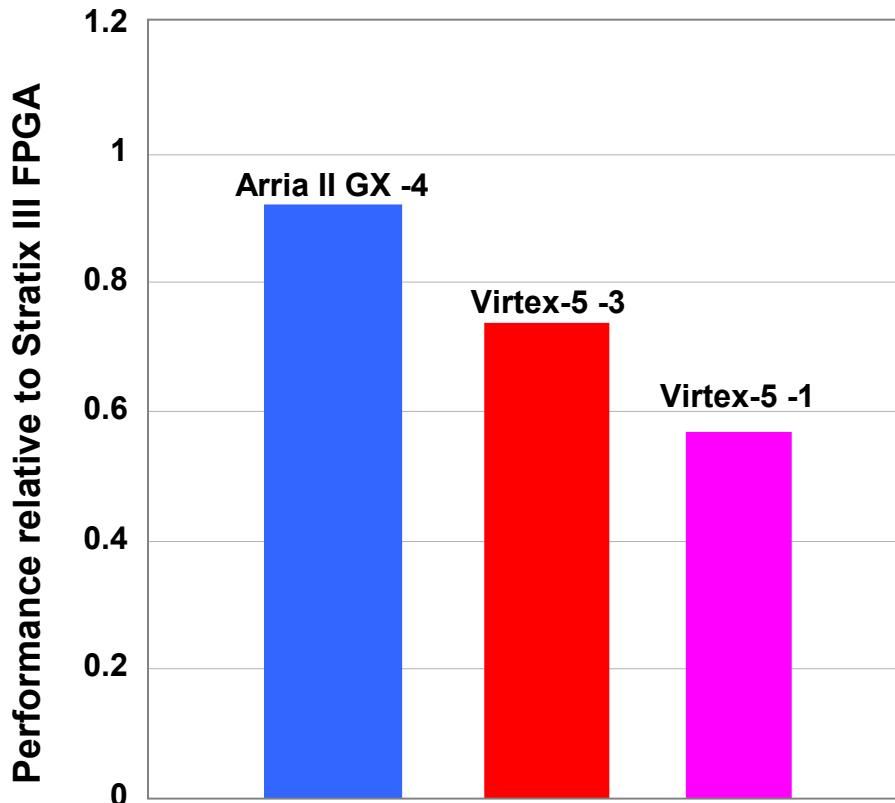
***Best solution for 3-Gbps applications***

# Industry's Most Advanced FPGA Fabric

- High-performance FPGA fabric based on proven 40-nm technology
  - Adaptive logic module (ALM): Efficient architecture from Stratix IV FPGAs
    - Improves device utilization
    - Compact logic closer together
    - Increases  $f_{MAX}$  performance



# Arria II GX Performance Advantages

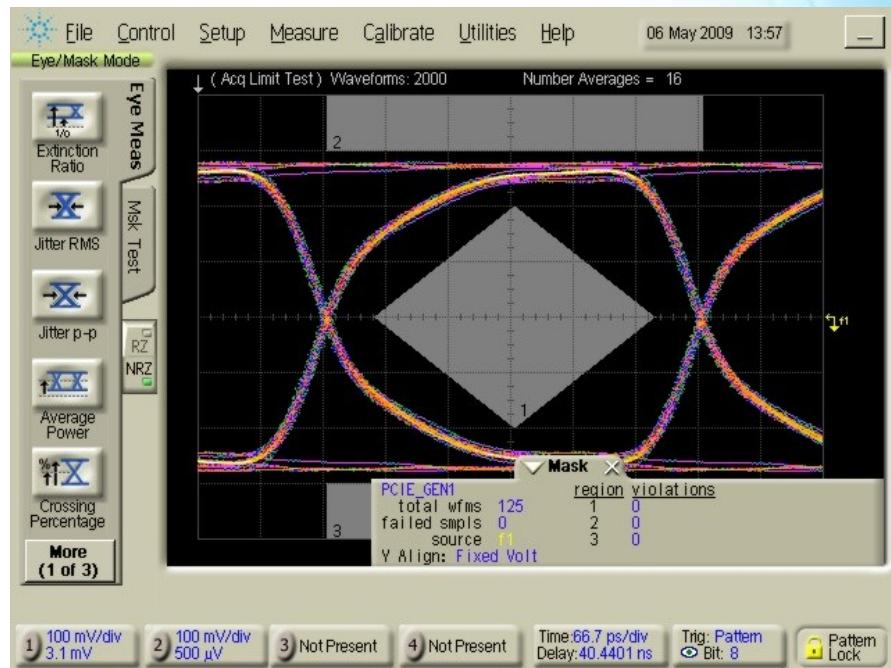


- Based on analysis of 60+ user designs
- Designs compiled multiple times in Quartus II and ISE
  - Using all available settings to maximize performance
  - Fmax increased for each iteration until it can no longer be met

*On average, Arria II GX FPGAs are 25% faster than Virtex-5 FPGAs*

# Arria II GX Transceiver Technology

- Proven 40-nm technology
- Optimized for cost and power
  - <100mW per channel
- Up to 16 transceivers that support mainstream 3.75-Gbps protocols
- Excellent signal integrity
  - 1.59 ps random jitter

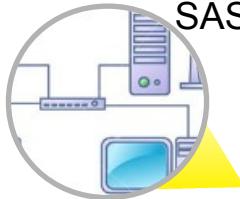


PCIe Gen1: Tx eye diagram, mask test

# Comprehensive, Robust Protocol Support

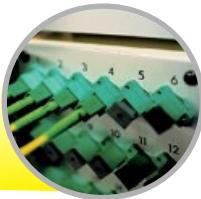
## Mainstream

PCI Express  
3G basic  
Gigabit Ethernet  
SATA  
SAS



## Wireline

Fibre Channel  
SerialLite II  
SGMII, SONET  
GPON, XAUI



## Wireless

CPRI  
OBSAI  
SRIO



**ALTERA**  
**Arria™ II GX**



## Broadcast

SD  
HD  
3G-SDI

Protocol	Data rate (Gbps)
ASI	0.27
Basic (proprietary)	0.6 - 3.75
CPRI	0.6144, 1.2288, 2.4576, 3.072
10G Ethernet (XAUI)	3.125
Gigabit Ethernet	1.25
GPON	1.244 uplink, 2.488 downlink
HiGig+	3.75
OBSAI	0.768, 1.536, 3.072
PCI Express Gen1	2.5
PCI Express Cable	2.5
SAS	1.5, 3
SATA	1.5, 3
SDI SD/HD	0.27 / 1.485
3G-SDI	2.97
SerialLite II	0.6 - 3.75
Serial RapidIO®	1.25, 2.5, 3.125
SONET OC-3/OC-12/OC-48	0.155, 0.622, 2.488

# Efficient Internal Memory Configurations

Memory type	Applications	Benefits
M9K  9K bits	<ul style="list-style-type: none"><li>■ General purpose memory in RAM, ROM, or FIFO configurations</li><li>■ Large HD video buffers</li><li>■ Packet processing</li></ul>	<ul style="list-style-type: none"><li>■ Fast 390-MHz performance</li><li>■ More data bits for larger buffering</li><li>■ Low-power operation</li></ul>
MLAB  640 bits	<ul style="list-style-type: none"><li>■ Shift registers</li><li>■ Filter delay lines</li><li>■ DSP</li></ul>	<ul style="list-style-type: none"><li>■ Placed close to logic for faster timing</li><li>■ More data ports for greater bandwidth</li><li>■ Efficient memory usage for small buffers</li></ul>

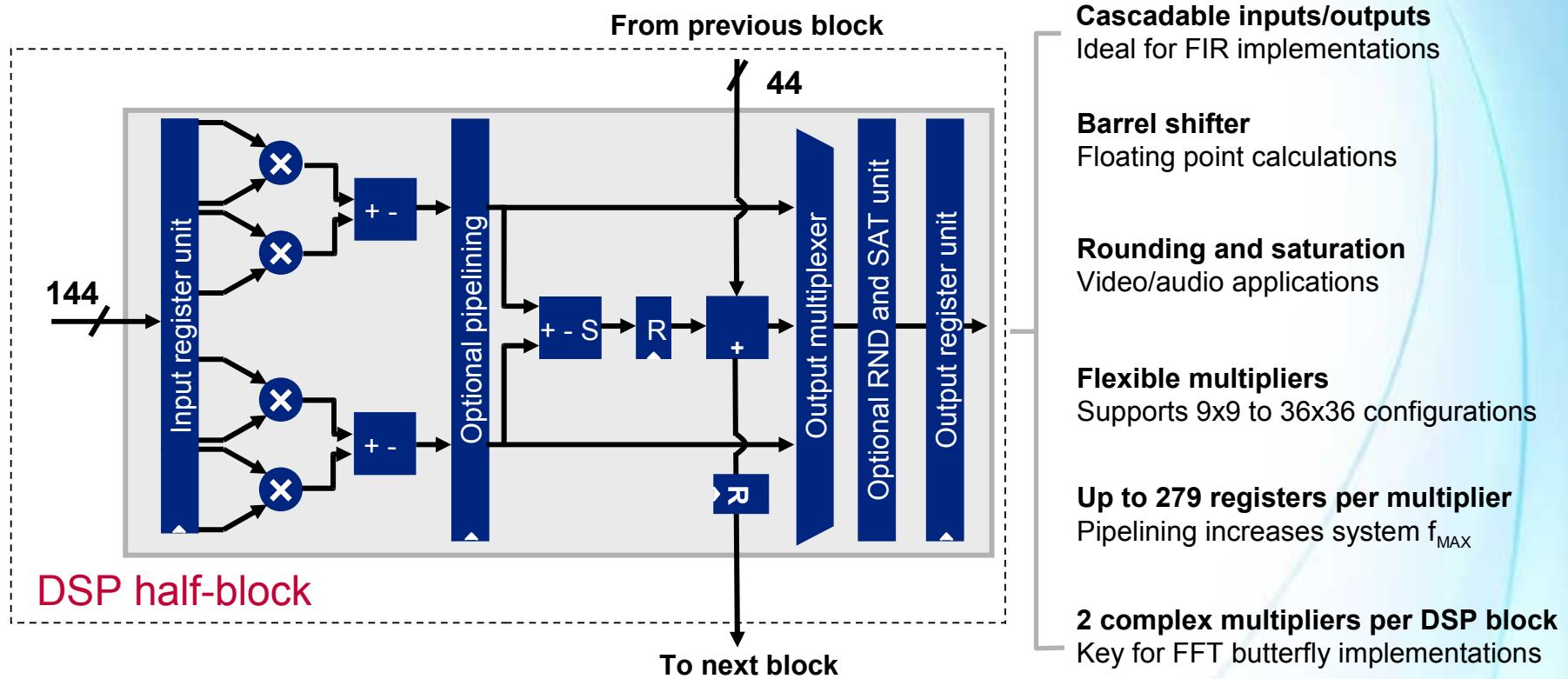
***Optimized block size for maximum efficiency***

# Memory Feature Summary

Feature	MLAB	M9K
Performance	350 MHz	390 MHz
Simple dual-port	✓	✓
True dual-port		✓
Parity	✓	✓
Packed mode		✓
ECC <sup>(1)</sup>	✓	✓
Low-power mode	✓	✓
Shift register	✓	✓
FIFO	✓	✓
Initialization	✓	✓
Mixed clock	✓	✓
Byte enable	✓	✓
Address clock enable	✓	✓

Note: (1) Soft ECC implementation

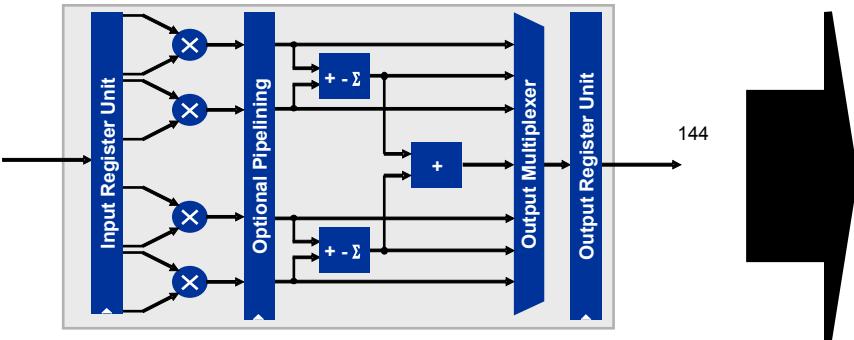
# Advanced DSP Blocks



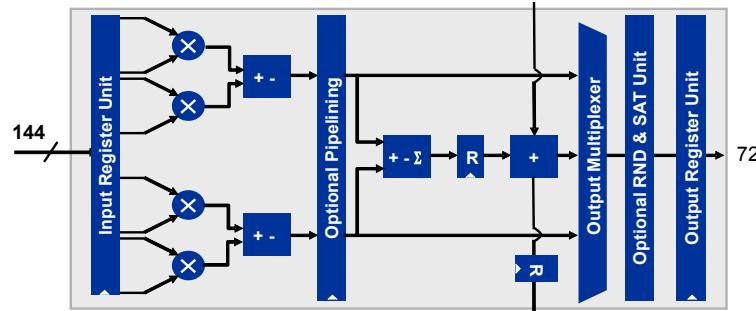
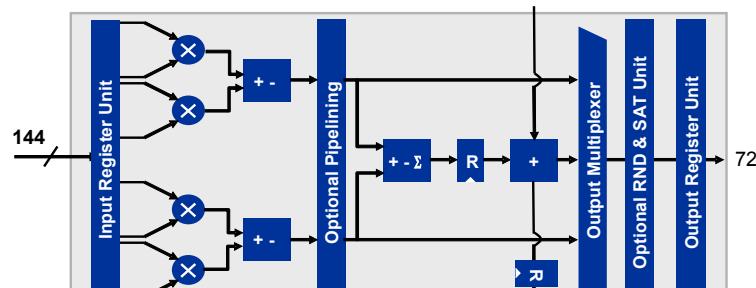
***Optimized memory to multiplier ratio  
(1.3 M9K block for each multiplier)***

# DSP Block Evolution

Arria GX



Arria II GX



- Basic multiplier modes
    - 8 x (9x9)
    - 4 x (18x18)
    - 1 x (36x36)
    - 1 x complex (18x18)
  - Accumulation
    - 2 x acc
  - Rounding
    - 16-/32-bit biased
  - Saturation
    - 32-bit asymmetrical
  - Barrel shifter
    - Partial support
- 
- Basic multiplier modes
    - 8 x (9x9)
    - 6 x (12x12)
    - 4 x (18x18)
    - 4 x (18x36)
    - 2 x (36x36)
    - 2 x complex (18x18)
  - Multiply and sum modes
    - 4 x sum of two (18x18)
    - 2 x sum of four (18x18)
  - Accumulation
    - 2 x acc
  - Cascade modes
    - Input cascade
    - Output cascade
  - Rounding
    - Unbiased and biased
  - Saturation
    - Asymm and symmetrical
  - Barrel shifter
    - Arithmetic, logical, and rotation

# Arria II GX Multiplier Capabilities

	Device	LE	Multipliers				
			9x9	12x12	18x18	36x36	18x18 complex
Arria II GX	EP2AGX20	16K	112	84	56	14	14
	EP2AGX30	27K	288	216	144	36	36
	EP2AGX45	45K	456	342	228	57	57
	EP2AGX65	63K	624	468	312	78	78
	EP2AGX95	94K	888	666	444	111	111
	EP2AGX125	124K	1152	864	576	144	144
	EP2AGX190	190K	1312	984	656	164	164
	EP2AGX260	257K	1472	1104	736	184	184

**Arria II GX DSP block can be optimized for different multiplier sizes**

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# Support for All Popular External Memories

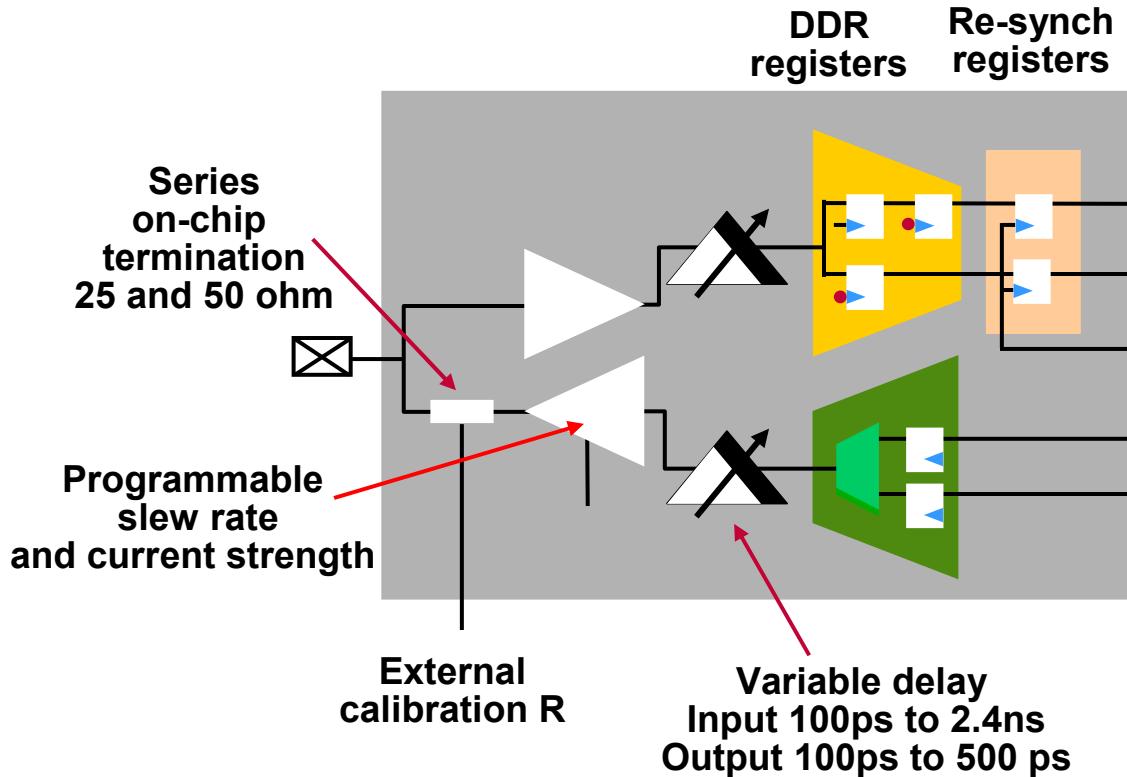
Memory standard	I/O standard	Data group sizes	Max frequency (MHz)	Max data rate (Mbps)	Max bus width	DIMM support?
DDR SDRAM	2.5V SSTL	8, 16	200 (I)	400 (I)	72 bits	Yes
DDR2 SDRAM	1.8V SSTL	8, 16	300 (C) 267 (I)	600 (C) 533 (I)	72 bits	Yes
DDR3 SDRAM	1.5V SSTL	8, 16,	300 (C)	600 (C)	72 bits	No
QDR II SRAM	1.5V HSTL	9, 18, 36	250 (I)	1,000 (I)	36 Rd, 36 Wr	N/A

(C) Commercial temperature

(I) Industrial temperature

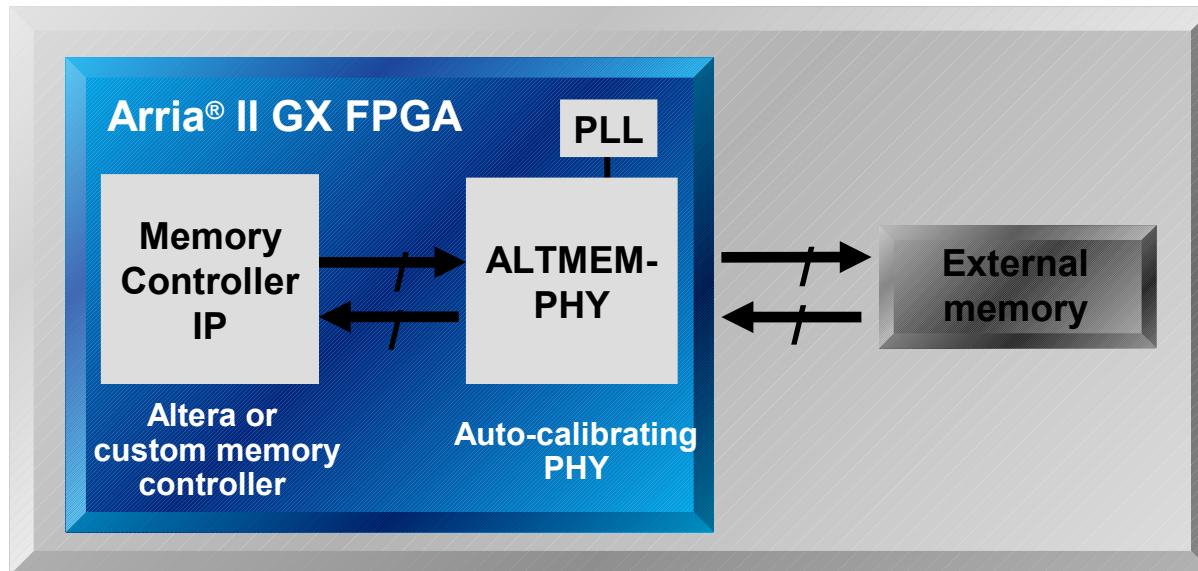
***Up to 80 Gbps of external memory bandwidth***

# Arria II GX Single-Ended I/O Architecture

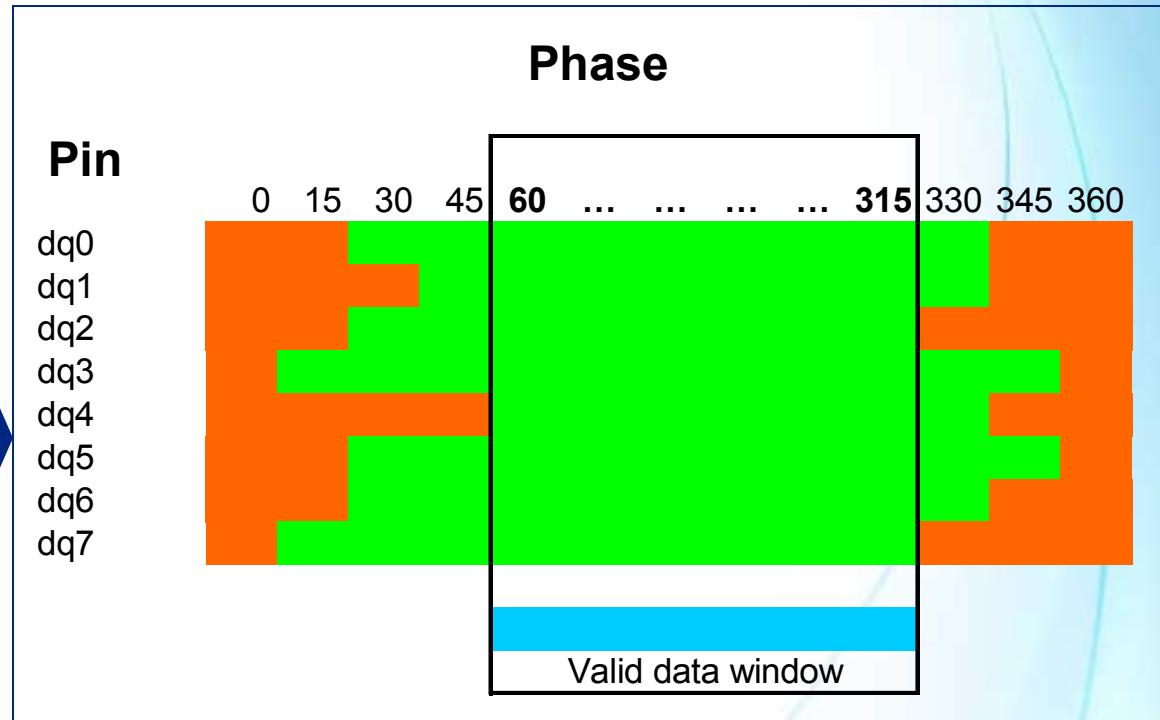
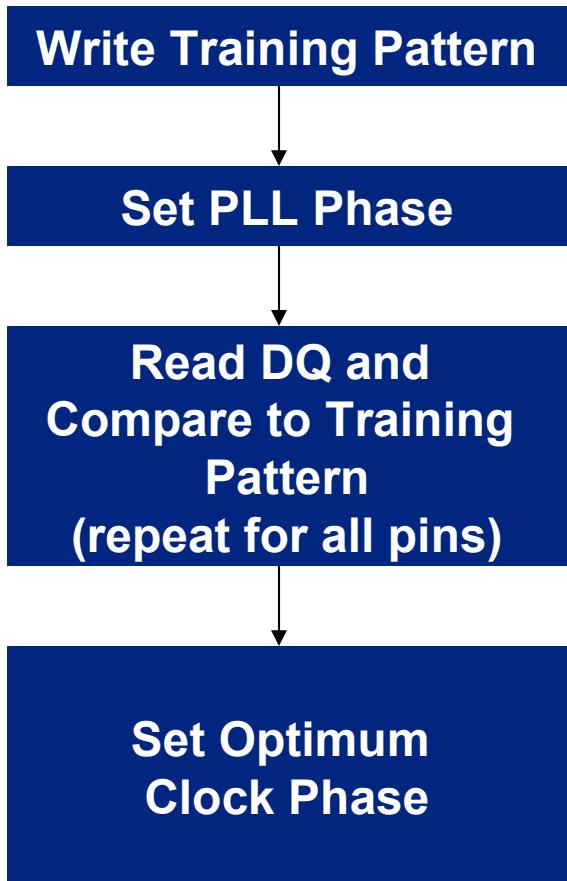


# Solution: Improve Reliability and Reduce Design Time with Self-Calibrating Interfaces

- Fast timing closure and higher reliability with auto-calibrating PHY
  - Periodic calibration for voltage and temperature variations
  - Reduces simulation and design time
  - Uninterrupted operation
- Use Altera's memory controller IP, or create your own



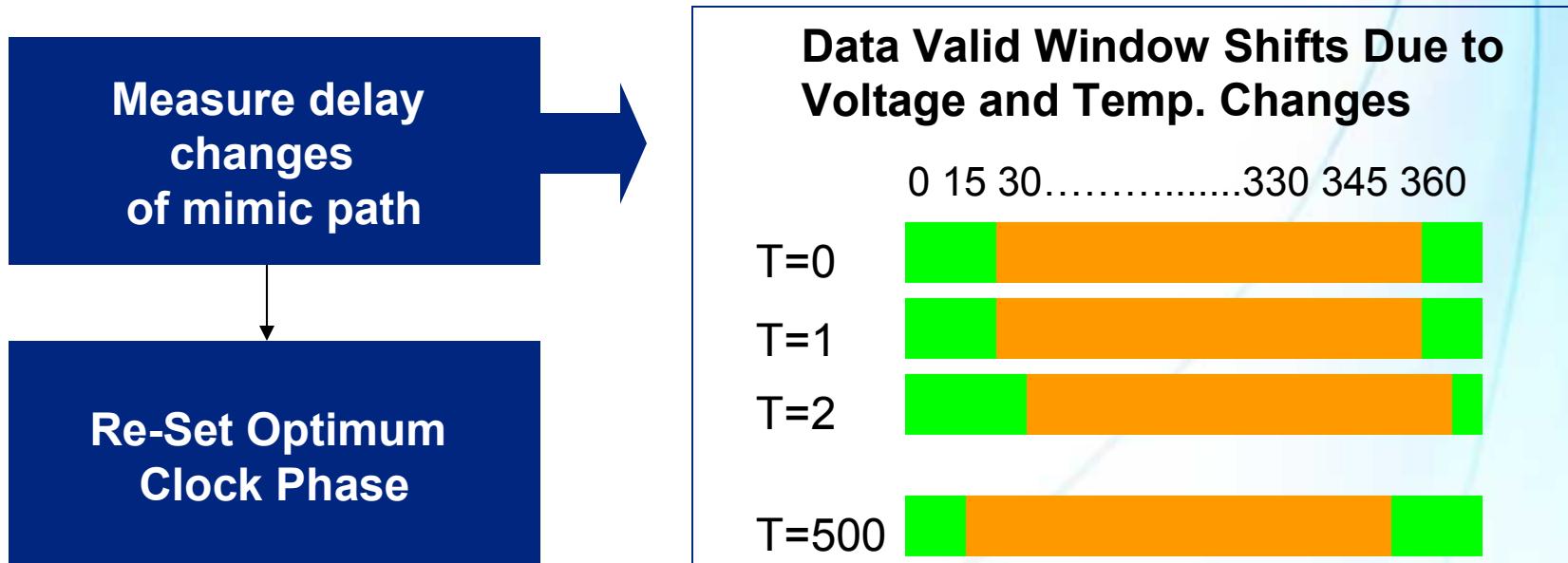
# Calibration at Startup



*PHY adapts to your system!*

# Periodic Calibration for Voltage and Temp

- Data capture and measurement of a representative mimic path delay every 128 ms
  - Path delay may change due to voltage and temperature changes
  - Assumption: Data Valid window drift due to temperature and voltage similar to delay change of representative path
- Dynamic phase adjustment to match the shifting data valid windows

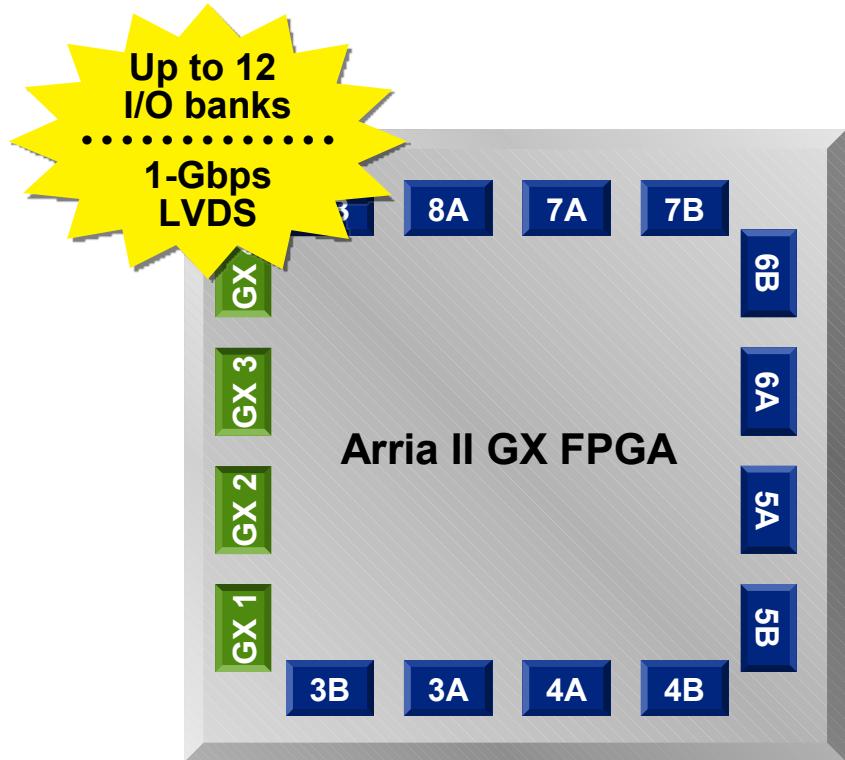


# Arria II GX Single-Ended I/O Support

I/O standard	Standard support	Input V <sub>CCIO</sub> (V)	Output V <sub>CCIO</sub> (V)
3.3V LVTTL/3.3V LVC MOS	JESD8-B	3.3/3.0/2.5	3.3
3.0V LVTTL/3.0V LVC MOS	JESD8-B	3.3/3.0/2.5	3.0
2.5V LVTTL/LVC MOS	JESD8-5	3.3/3.0/2.5	2.5
1.8V LVTTL/LVC MOS	JESD8-7	1.8/1.5	1.8
1.5V LVC MOS	JESD8-11	1.8/1.5	1.5
1.2V LVC MOS	JESD8-12	1.2	1.2
3.0V PCI	PCI Rev 2.2	3.0	3.0
3.0V PCI-X (1)	PCI-X Rev 1.0	3.0	3.0
SSTL-2 Class I and Class II	JESD8-9B	3.3/3.0/2.5 (1)	2.5
SSTL-18 Class I and Class II	JESD8-15	3.3/3.0/2.5 (1)	1.8
SSTL-15 Class I	-	3.3/3.0/2.5 (1)	1.5
HSTL-18 Class I and Class II	JESD8-6	3.3/3.0/2.5 (1)	1.8
HSTL-15 Class I and Class II	JESD8-6	3.3/3.0/2.5 (1)	1.5
HSTL-12 Class I and Class II	JESD8-16A	3.3/3.0/2.5 (1)	1.2

Note (1): Single-ended SSTL/HSTL input buffers are powered by pre-driver Vcc pins (VCCPD)

# Flexible I/O Connectivity



Transceiver I/O bank

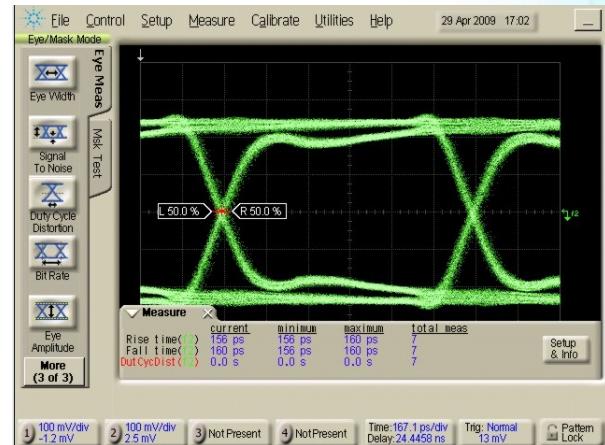
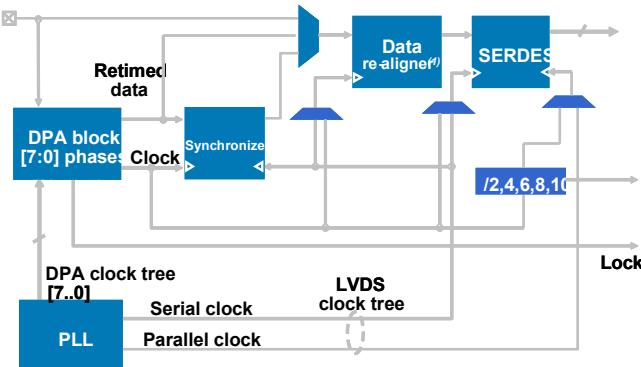
General I/O bank

- Robust single-ended I/Os
  - Support all popular standards such as SSTL, HSTL, etc.
  - Up to 612 user I/Os
  - Adjustable slew rate, drive strength, and buffer delay
- High-speed differential I/Os
  - 150-Mbps to 1-Gbps data rates
  - Dynamic on-chip termination (OCT) saves power and space
  - Dynamic phase alignment (DPA) maximizes timing margin
  - Clock-data recovery (CDR) compensates skew

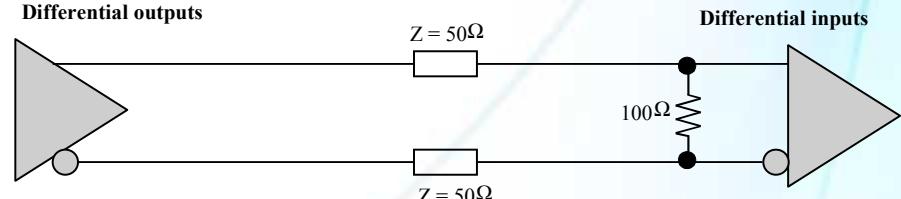
***Easily connect with multiple I/O standards***

# Differential LVDS I/O Buffer with Hard DPA Block

- Programmable pre-emphasis
  - Compensate for attenuation in trace lengths
  - On/off setting
- Programmable voltage output differential (VOD)
  - Adjust output eye height to optimize for trace length and power consumption
- Differential on-chip termination
- Hard DPA block
- Eliminates skew requirements



Arria II GX LVDS eye diagram at 1 Gbps

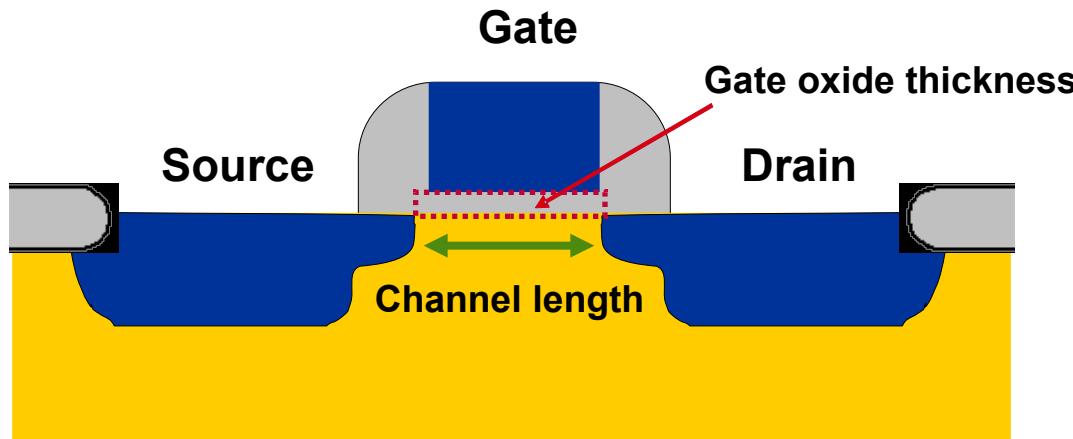


# Design Protection With AES Encryption

- Configuration bitstream encryption
  - Advanced encryption standard (AES)
  - 256-bit key
  - Both volatile and non-volatile key storages
- Protection against:
  - Copying
  - Reverse-engineering



# Low-Power Process and Silicon Optimizations

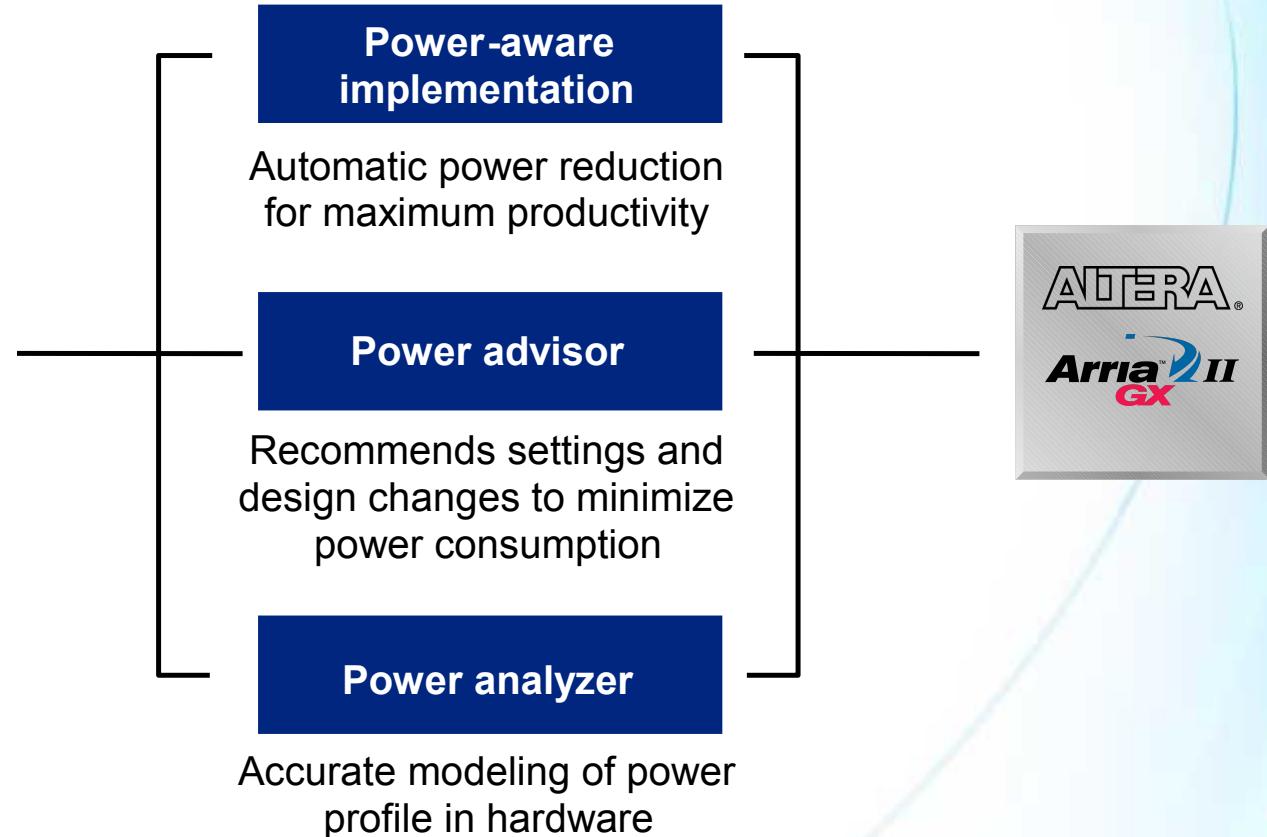


Optimization	Benefit
TSMC 40-nm GLP process	Proven lower power process technology
Multiple threshold voltages, variable channel length, and gate oxide thicknesses	Lower power for non speed-critical transistors
Strained silicon	Increases performance while reducing power consumption
Core voltage reduced from 1.2V to 0.9V	Reduces dynamic power

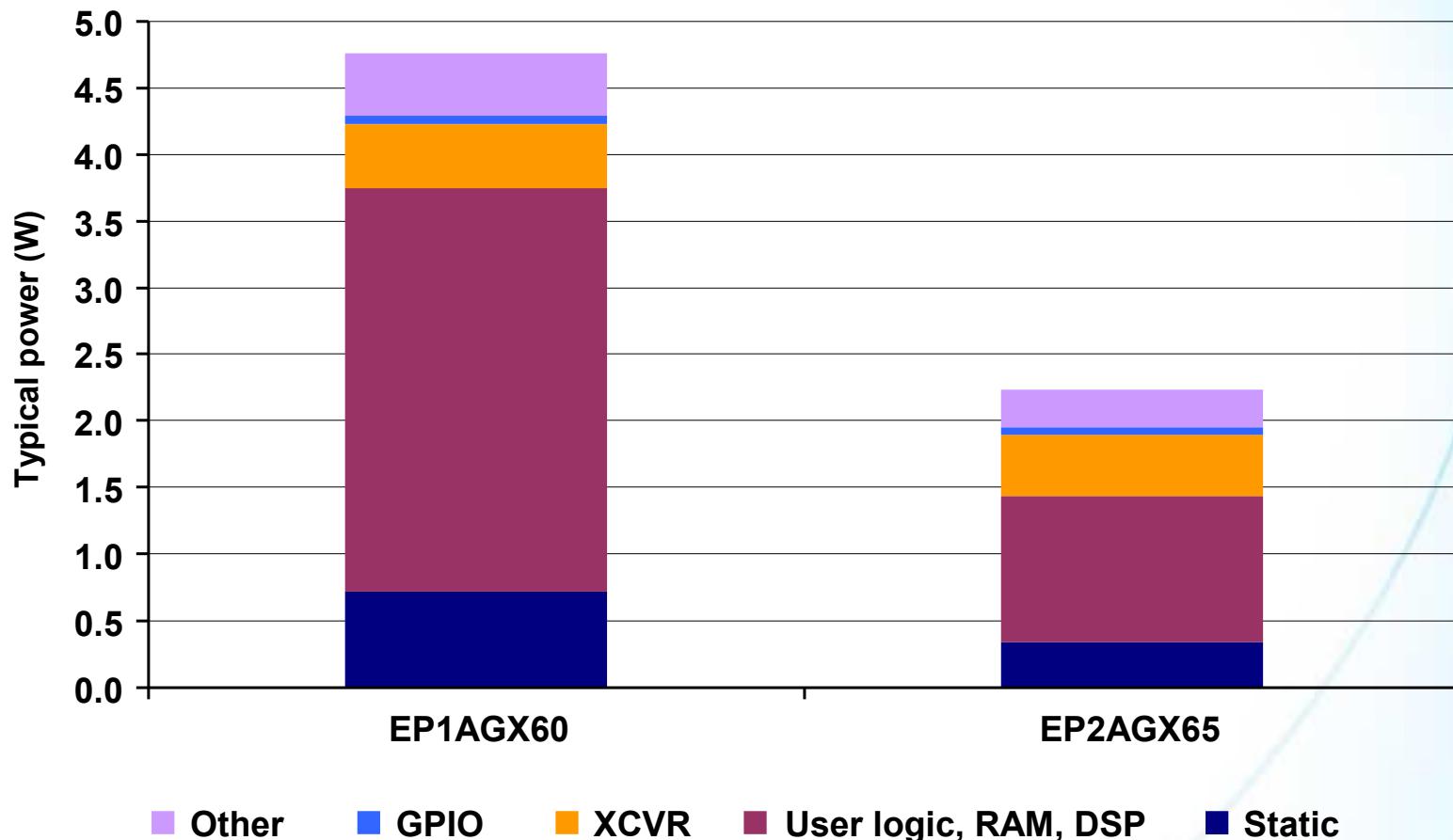
# Advanced, Accurate Power Analysis Tools



**Quartus II software**  
Increase productivity  
with fastest compile  
times in the industry



# Meet Your Power Budgets Without Compromise



**Half the power of previous generation**

# Design Examples to Get You Started Now

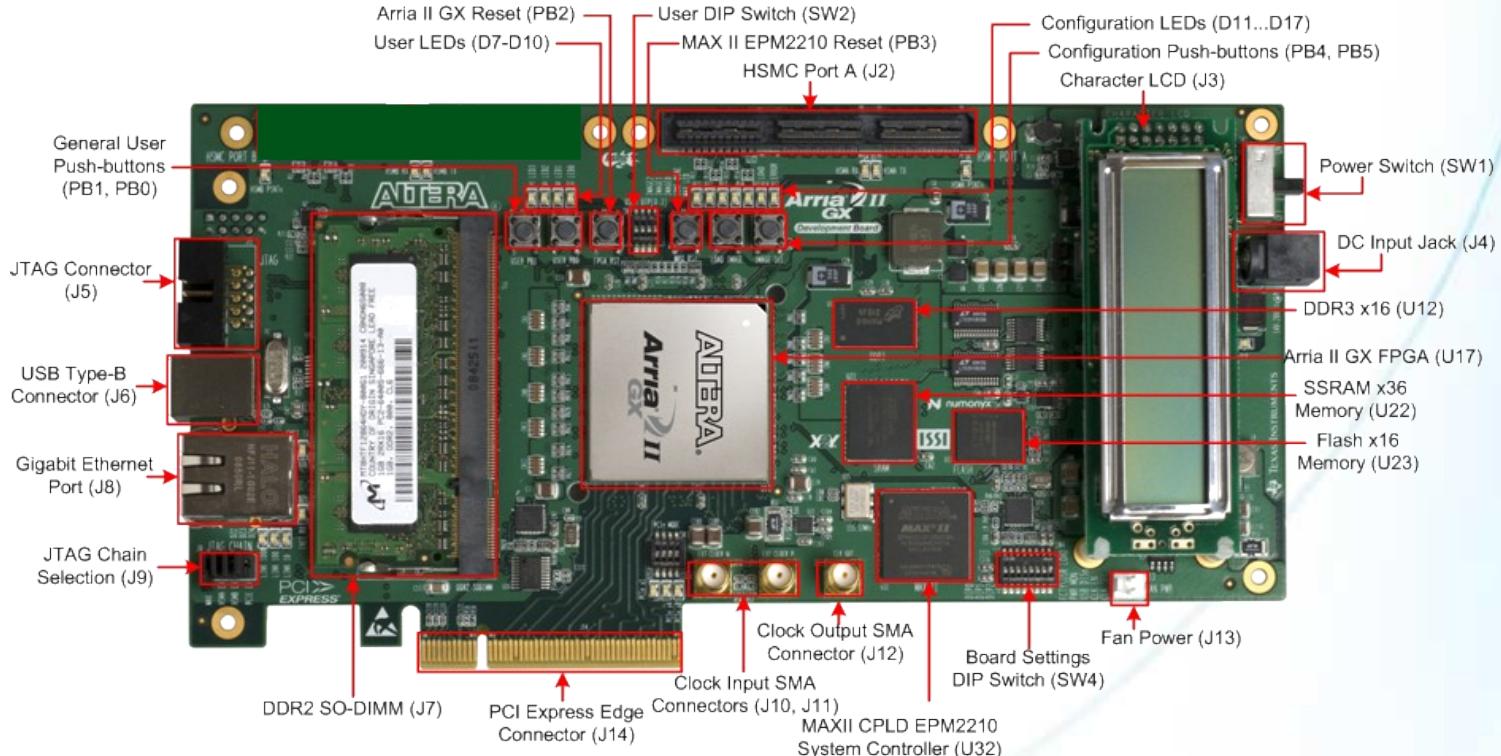
Protocols/applications	IP/design examples
PCIe Gen1	PCIe to DDR2 bridge
PCIe Gen1	High-performance PCIe to DMA
SDI	Triple-rate SDI
Ethernet	10 Gigabit Ethernet
Memory controller	DDR2 QDR II
Wireless reference designs	WiMAX digital up/down conversion, crest factor reduction, digital pre-distortion
Broadcast reference designs	Color space converter, chroma resampler, 2D median filter, deinterlacer

- Examples include: HDL code, testbench, timing constraints, documentation
- Hardware verified reference designs available with Arria II GX Development Kit

***[Click here to see these and other design resources](#)***

# Arria II GX Development Kit

- \$1,495 list price
  - Ordering code = DK-DEV-2AGX125N
  - 125K Logic Element, 40-nm FPGA
  - F1152 1.0mm BGA package
  - 12 Transceiver I/Os up to 3.75 Gbps
- PCIe long form factor
- HSMC loop-back & debug daughter-cards
- Quartus® II, Dev Kit Evaluation Edition
  - 12 month license
- Complete documentation & ref. designs
  - Pre-loaded embedded processor design



# Board and Transceiver Design/Debug Tools

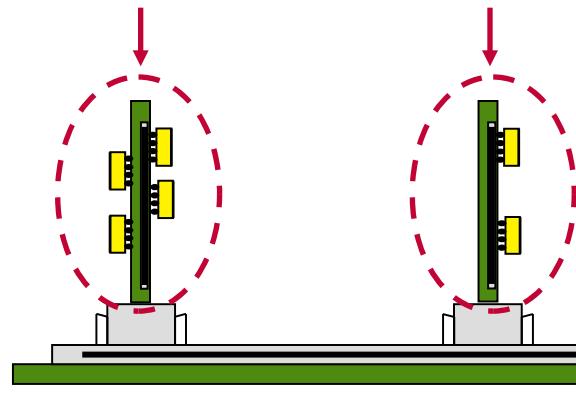
Resource/applications	Explanation
Protocol IP packs (PCIe, SRIO, CPRI, SATA, SDI, and GbE)	Includes “getting started” guide, design examples/reference designs, training, sell sheet, interoperability testing
Transceiver design white paper	Quick start guide covering transceiver design and debug techniques for Arria II GX FPGAs
SSN analyzer (Quartus II software)	Estimate and prevent SSN effects that may cause functional and/or timing failures on the PCB board
Power distribution network (PDN) tool	Optimize board-level PDN
General board design guidelines	Optimize your board for required performance and cost, and avoid board re-spins
Simulation	IBIS, HSPICE models
ACJTAG	Supports board-level transceiver diagnostics

***Move quickly from design to production***

# Transceiver Design With Arria II GX FPGA

## Board design

- PDN tool
- Design guidelines
- Single-chip solution
- <100mW per channel



## System upgrades

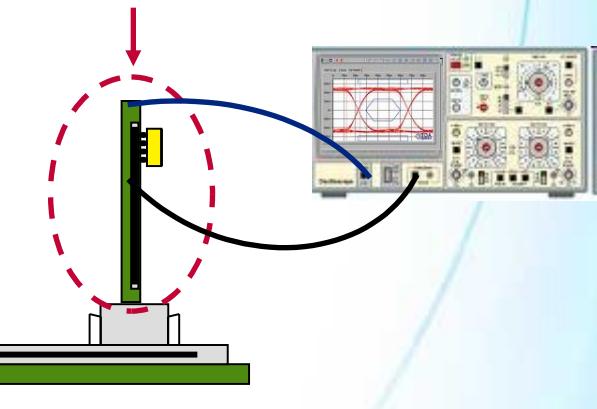
- Multiple protocols per channel
- Multiple data rates per channel

## Signal quality

- Dynamic reconfiguration
- Pre-emphasis
- Equalization

## Time to market

- SSN analyzer
- PCI Express hard IP
- ACJTAG
- SOPC Builder
- MegaWizard™

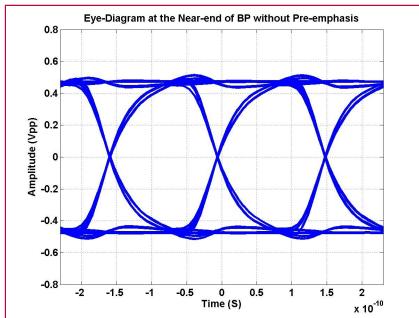


## ■ Supporting collateral:

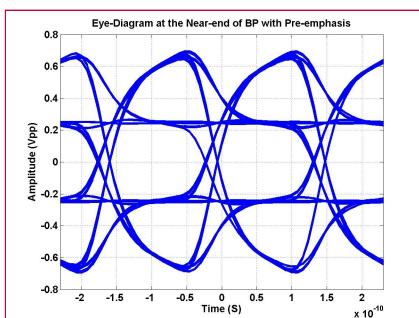
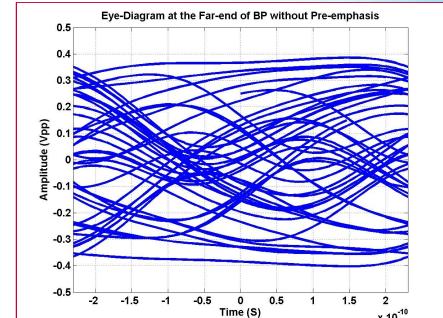
- Transceiver design guidelines
- Tutorials and white papers
- Video demonstration and training

***Transceiver design with ease***

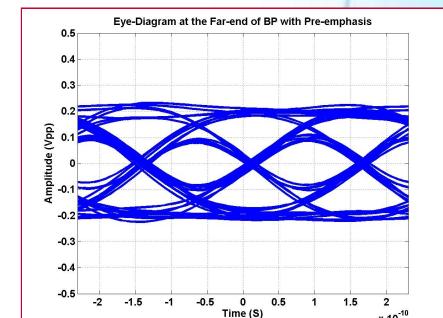
# Transmitter Pre-Emphasis



Without pre-emphasis



With pre-emphasis



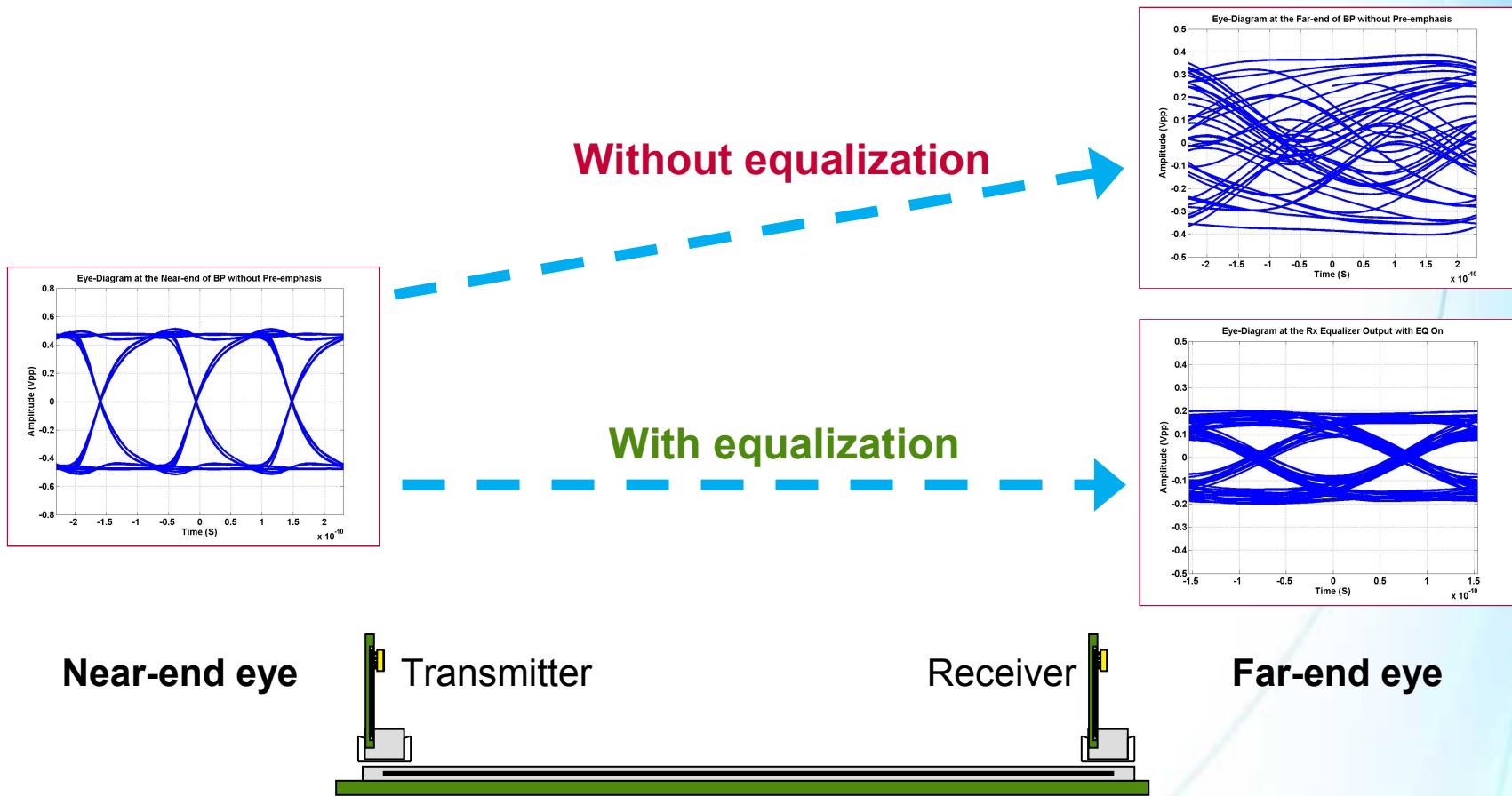
Near-end eye



Far-end eye

***Pre-emphasis maximizes data eye opening at receiver***

# Receiver Equalization



**Rx adjusts equalizer for optimal signal integrity**

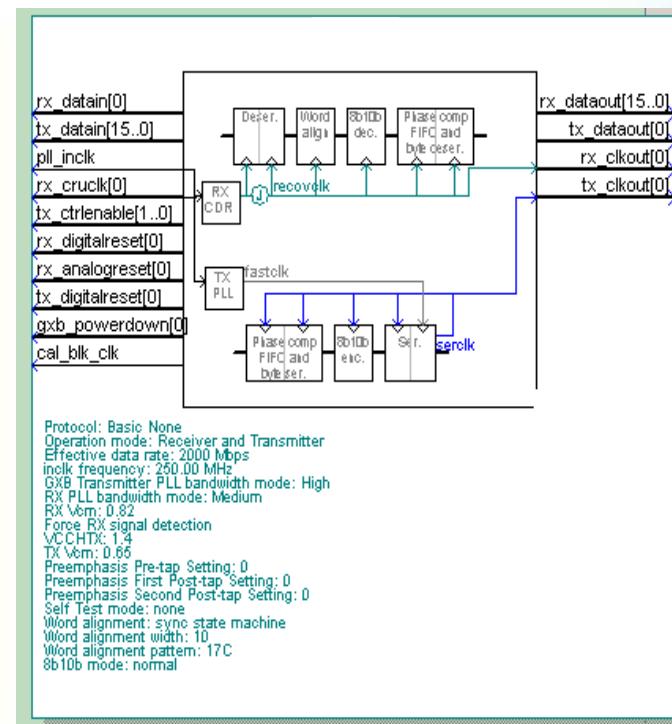
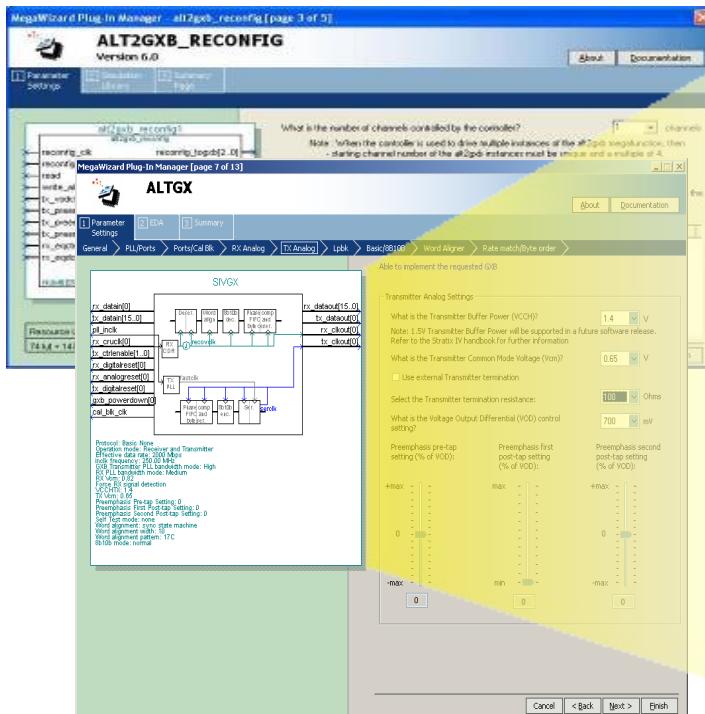
# Dynamic Reconfiguration Minimizes In-Field Downtime

- Transceiver dynamic reconfiguration
  - Adjust to new data rates, protocols, and PMA settings without affecting adjacent channels
- Board-level benefits
  - Eliminates the need for multiple ASSPs
  - Reduces board complexity, size, and cost
- System-level benefits
  - Continuous backplane signal integrity optimization minimizes bit-error ratio
  - Enables remote upgrades without downtime

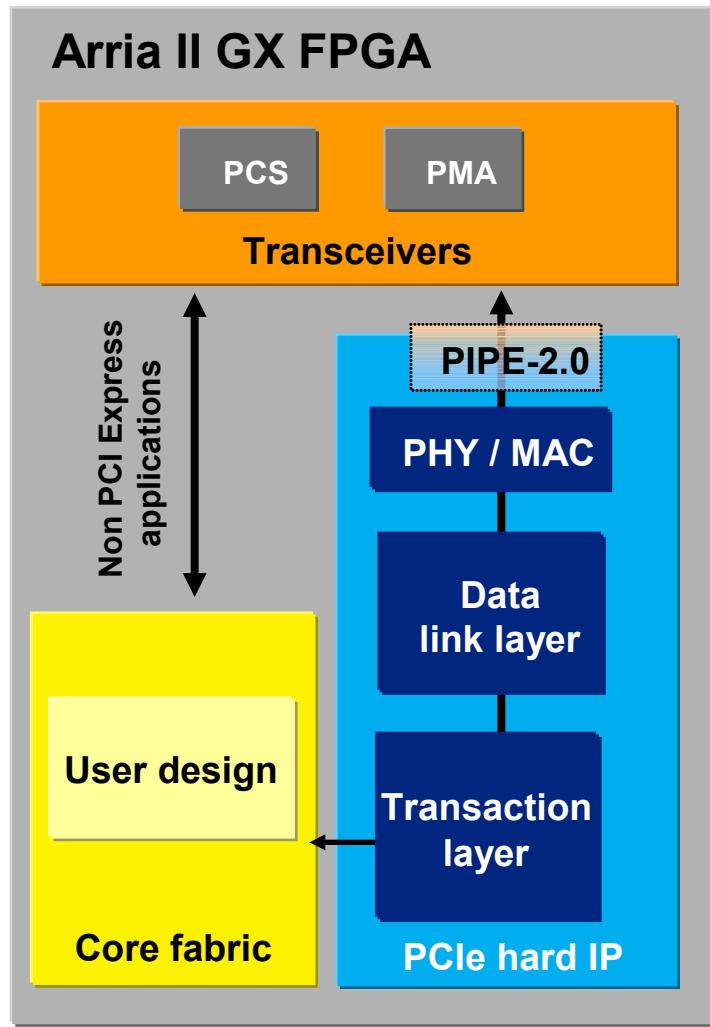
***Support multiple protocols with one port***

# Easy Design Entry with ALTGX MegaWizard

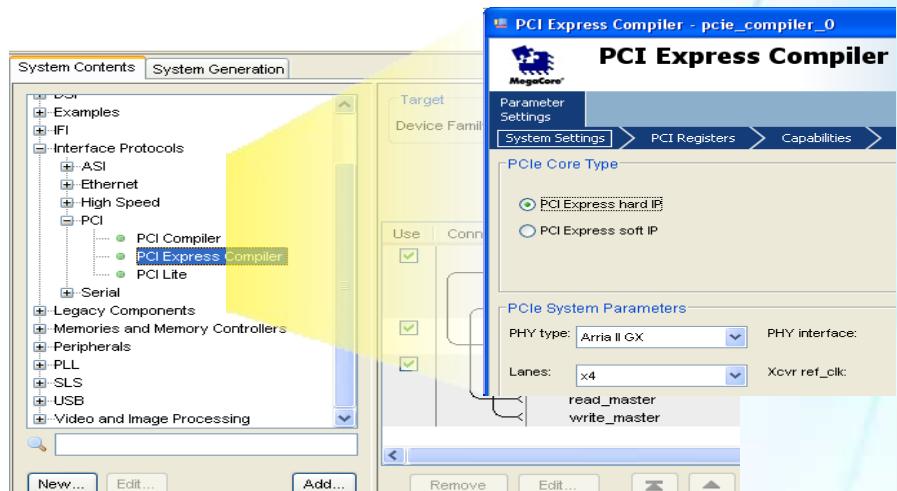
- Easy-to-use GUI interface
- Select target protocol and optimal settings for your design needs
- “Drop-in” transceivers into your design



# Complete a PCIe Design in 45 Minutes



- Built-in, pre-verified PCIe v1.1 hard IP
- Guaranteed timing
- Flexible x8, x4, x2, x1, rootport and endpoint configurations
- SOPC Builder ready
- Reduces cost and area
  - 15K LEs saved, no license fees required
- View webcast [here](#)



# Arria II GX Family Plan

Device	Equiv LEs	RAM Mbits/ M9K blocks	Total MLAB memory (Mbits)	18 X 18 multipliers	Transceivers @ 3.75 Gbps	PLLs	Tx PLLs	CIs
EP2AGX45	45K	2.9 / 319	0.6	228	8	4	4	32
EP2AGX65	63K	4.4 / 495	0.8	312	8	4	4	32
EP2AGX95	94K	5.5 / 612	1.2	448	12	6	6	40
EP2AGX125	124K	6.6 / 730	1.6	576	12	6	6	40
EP2AGX190	190K	7.6 / 840	2.4	656	16	6	8	40
EP2AGX260	256K	8.5 / 950	3.2	736	16	6	8	40

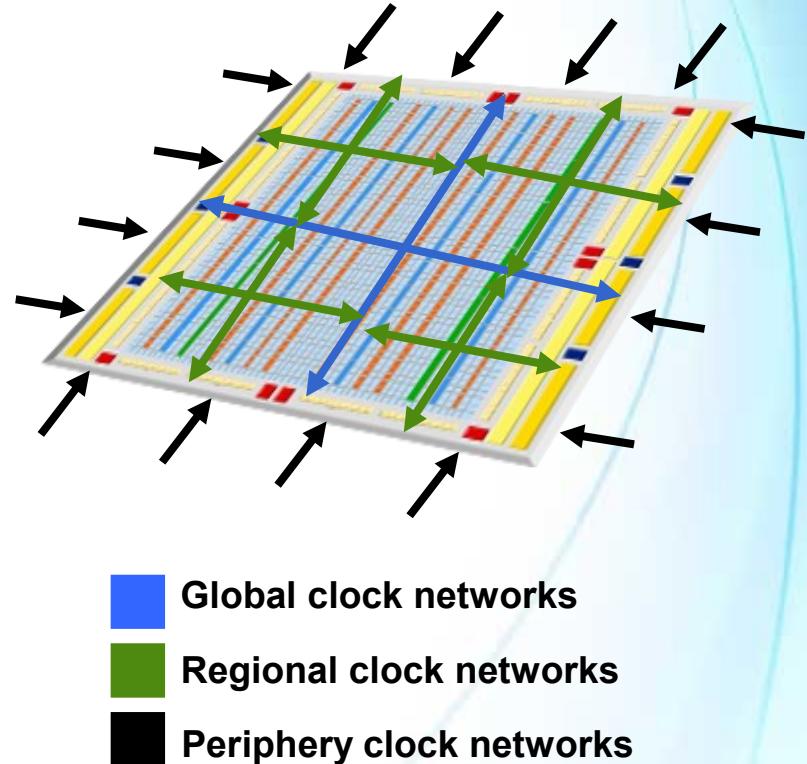
# More Clock Resources for Your Design

## ■ Hierarchical clock networks

- Support up to 148 clock domains
  - 16 global networks
  - 48 quadrant networks
  - 84 periphery networks
- Drive clocks from anywhere
  - Pins, PLLs, or logic

## ■ Effective PLL clock management

- Up to 6 low-jitter PLLs
- 7 independent clock outputs per PLL
- Cascade support
- Dynamically reconfigurable
- Easy setup with MegaWizard



***Confidently manage clock domains***

# Arria II GX Package Offerings

Device	U358	F572	F780	F1152
	0.8 mm 17 x 17	1.0 mm 25 x 25	1.0 mm 29 x 29	1.0 mm 35 x 35
EP2AGX45	156 (32,4)	252 (56,8)	364 (84,8)	
EP2AGX65	156 (32,4)	252 (56,8)	364 (84,8)	
EP2AGX95		260 (56,8)	372 (84,12)	452 (104,12)
EP2AGX125		260 (56,8)	372 (84,12)	452 (104,12)
EP2AGX190			372 (84,12)	612 (144,16)
EP2AGX260			372 (84,12)	612 (144,16)



Number of I/Os (LVDS, number of transceivers)

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