wavefront SEMICONDUCTOR

AL1201
24-bit Digital-to-Analog Converter

ClockEZ™ DAC

AL1201

General Description

The AL1201 is a 24-bit sigma-delta stereo digital-to-analog audio converter using Wavefront's ClockEZ™ technology. With dynamic range of 107dB, simplified interface, and low power consumption, the AL1201 (and its companion AL1101 ADC) is a best-in-class solution for 44.1kHz and 48kHz applications.

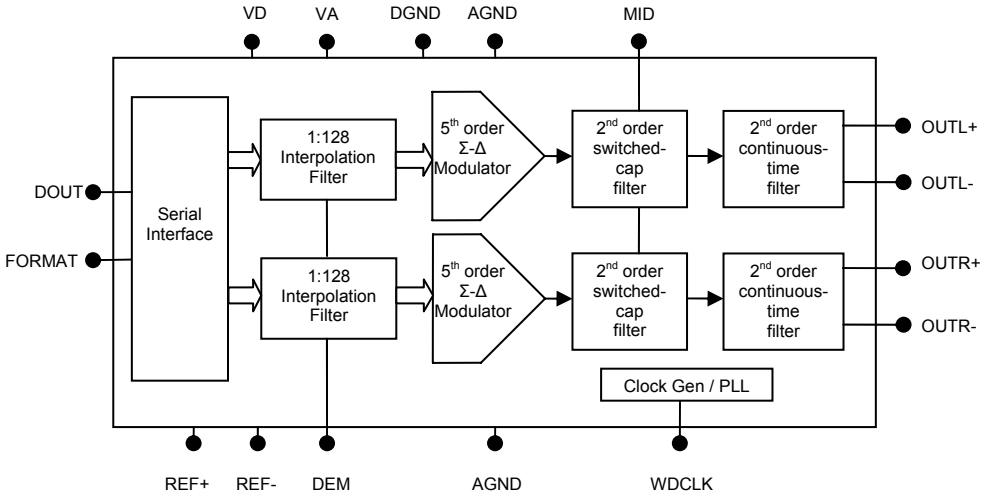
Applications

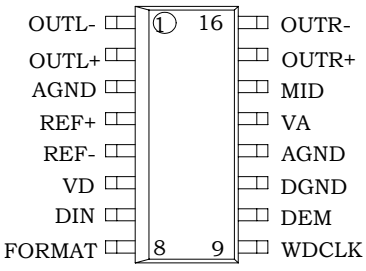
- Digital Mixing Boards
- Signal Processors
- Digital Effects Boxes
- Digital Recorders
- Computer Sound Boards
- Karaoke Systems
- Car Audio Systems
- CD audio

Features

- 24-bit conversion
- 107dB dynamic range (A-wt)
- 0.003% THD at full-scale output
- ClockEZ™ circuitry: internal PLL derives all necessary timing signals from one external Fs clock
- 128X oversampling, 5th order 1-bit Δ-Σ modulator
- 2nd order switched cap filter and 2nd order continuous-time filter on chip
- sample rate: 24kHz to 55kHz
- selectable deemphasis (15μs/50μs at Fs=44.1kHz)
- serial input selectable: 32/24 bits/frame
- full scale differential output = +/-4V
- 5V operation

Block diagram and package





16 pin SOIC
150 mils wide

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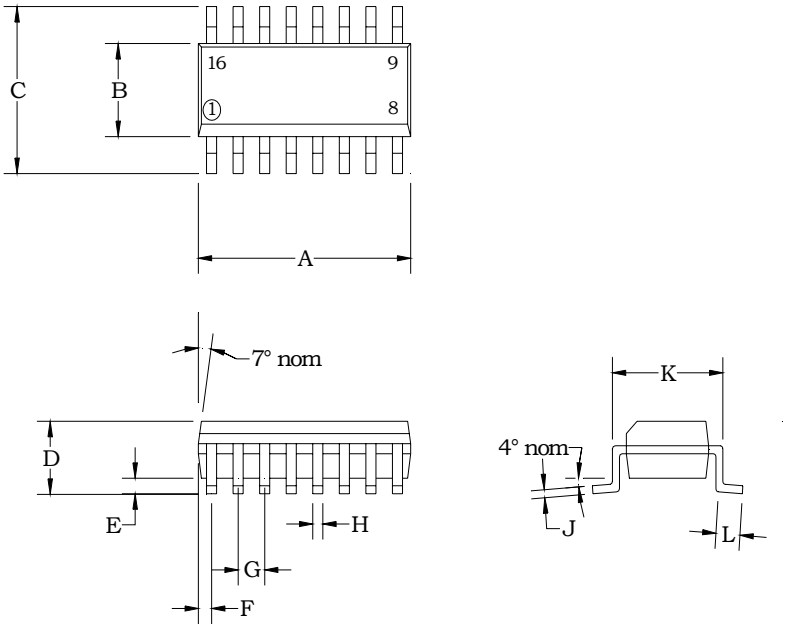
1201-0903

Pin Description

Pin #	Name	Pin Type	Description
1	OUTL-	OUTPUT	negative analog output, left channel
2	OUTL+	OUTPUT	positive analog output, left channel
3	AGND	GND	analog ground
4	REF+	PWR	positive reference, 5V, connect 0.1μF bypass cap to REF-
5	REF-	GND	negative reference, connect to GND
6	VD	PWR	digital supply, 5V, connect 0.1μF bypass cap to GND
7	DIN	INPUT	serial data input
8	FORMAT	INPUT	format select, 0=32 bits/frame, 1=24 bits/frame
9	WDCLK	INPUT	sample frequency wordclock, 24kHz<Fs<55kHz
10	DEM	INPUT	deemphasis select, 0=no deemphasis, 1=deemphasis
11	DGND	GND	digital ground
12	AGND	GND	analog ground
13	VA	PWR	analog supply, 5V, connect 0.1μF bypass cap to GND
14	MID	OUTPUT	mid reference, connect 0.1μF bypass cap to GND
15	OUTR+	OUTPUT	positive analog output, right channel
16	INR+	INPUT	negative analog output, right channel

Package Dimensions



Dimensions (Typical)	Inches	Millimeters
A	.389”	9.88
B	.154”	3.91
C	.236”	5.99
D	.100”	2.50
E	.008”	0.20
F	.025”	0.64
G	.050”	1.27
H	.017”	0.42
J	.011”	0.27
K	.170”	4.32
L	.033”	0.83

Note: Dimension “A” does not include mold flash, protrusions or gate burrs.

Recommended Operating Conditions

(GNDA=GNDD=0V)

Parameter	Comments	Min	Typ	Max	Units
VA	analog supply voltage	4.5	5.0	5.5	V
VD	digital supply voltage	4.5	5.0	5.5	V
T_a	ambient temperature	0	25	70	deg C
Fs	sample frequency	24	48	55	kHz
R_{load}	differential load resistance	12			kΩ

Analog Characteristics

(Ta=25°C, VA=VD=V_{REF}=+5V, Fs=48kHz, input=1kHz 24-bit data, measurement bandwidth=20Hz-20kHz, unless otherwise specified)

Parameter	Comments	Min	Typ	Max	Units
Dynamic Range	output=-60dBFS (A-wt)		107		dB
THD+N	output=0dBFS		-90		dB
	output=-20dBFS		-84		dB
	input=-60dBFS		-44		dB
Crosstalk	output=-0dBFS		-118		dB
Output voltage	[IN+] - [IN-] fullscale		+/-4.0		V
	interchannel match		0.05		dB
	differential DC offset		1		mV
	common mode DC bias		2.5		V
Max. output current			+/-0.4		mA
Output impedance	differential		3		Ω
Power Supply Current	analog (I_A)		28		mA
	digital (I_D)		6		mA
REF current	I_{REF} [2]		190		μA
Power Consumption			170		mW
Gain Error	REF+ held at 5V			+/-0.69	%
PSRR	REF+ held at 5V		70		dB

Note 1: Output voltage scales linearly with REF potential ([REF+]-[REF-]).
Note 2: REF current scales linearly with Fs.

Combined Digital and Analog Filter Characteristics

(Ta=25°C, VA=VD=V_{REF}=+5V, Fs=48kHz)

Parameter	Comments	Min	Typ	Max	Units
Passband	+/-0.1dB bandwidth [1]	0		21.77k	Hz
	Ripple			+/-.007	dB
Stopband	Frequency [1]	26.23			kHz
	Attenuation	-70			dB
Group delay			28.5		1/Fs
Deemphasis filter	Fs=44.1kHz				
	'pole' time constant		50		μs
	'zero' time constant		15		μs

Note 1: passband, stopband, and highpass frequencies scale with Fs.

Electrical Characteristics – Digital Pins

Parameter	Comments	Min	Typ	Max	Units
INPUTS (WDCLK, DIN, DEM, FORMAT)					
V_{IH}	Logical "1" input voltage	0.55VD			V
V_{OH}	Logical "0" input voltage			0.1VD	V
I_{IN}	input leakage current			1	μA
C_{IN}	input capacitance		5		pF

Applications Information

Serial Interface and Timing

The AL1201 receives its 2's complement serial data in a standard MSB-first format. Two bit-rates are allowed for. The 32-bits/frame rate (FORMAT low) is suitable for use in systems where a 256Fs master clock is present. The 24-bits/frame rate (FORMAT high) is convenient when interfacing with circuits where a 384Fs master clock is present.

The input sample period is defined between rising edges of the wordclock (WDCLK) input. Nominally, this is a 50% duty-cycle clock at frequency Fs, but it can be a pulse with Ts/256 < pulse-width < Ts (255/256); Ts=1/Fs. Left channel data is presented to the AL1201 with the rising edge of WDCLK, and right channel data is presented Ts/2 seconds later (when WDCLK falls if 50% duty cycle).

The serial bits are clocked into the AL1201 input registers on the falling edge of an internally generated bit clock (rising edge aligned with rising edge of WDCLK) that runs at 64Fs when FORMAT is low (32 bits/frame), or 48Fs when FORMAT is high (24 bits/frame). The input data should be valid +/-100ns from the falling edge of this internally generated clock. See timing diagram on next page.

Input Logic Levels

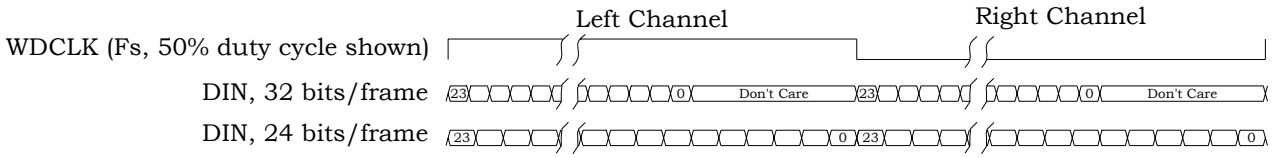
The AL1201 can properly receive input logical '1' voltages of .55VD. This means the AL1201 can interface directly with logic signals supplied from 3.3V systems. No special interface circuitry is required.

Internal Phase-Locked Loop (PLL)

The AL1201 contains an internal PLL that locks to the rising edge of WDCLK and produces all necessary high frequency clocks and timing signals to operate the device. This high quality PLL will reject any high-frequency jitter on the incoming wordclock (jitter rejection corner approx. 4kHz).

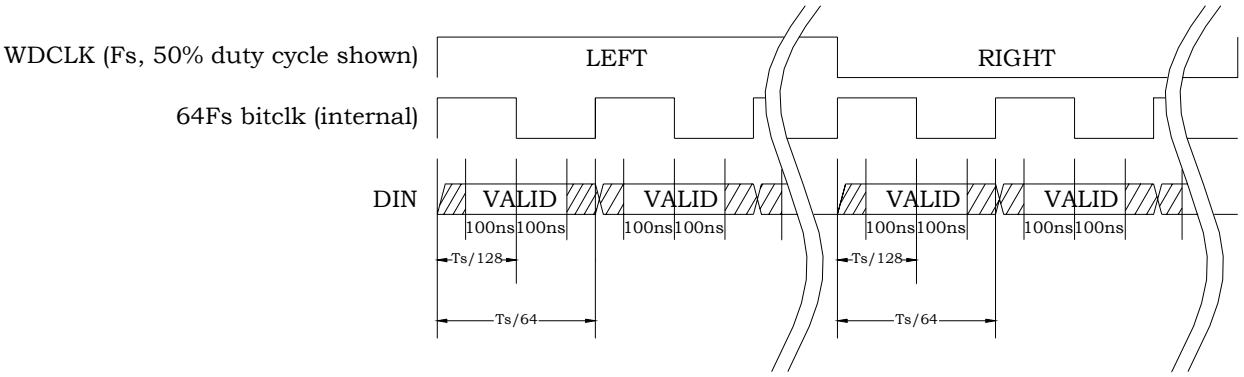
The PLL allows a simplified user interface and eliminates the need for running high frequency clocks on PCB traces to the AL1201. This reduces unwanted RF noise and coupling problems that can occur when these clocks are required as input pins for a device.

Serial Input Formats

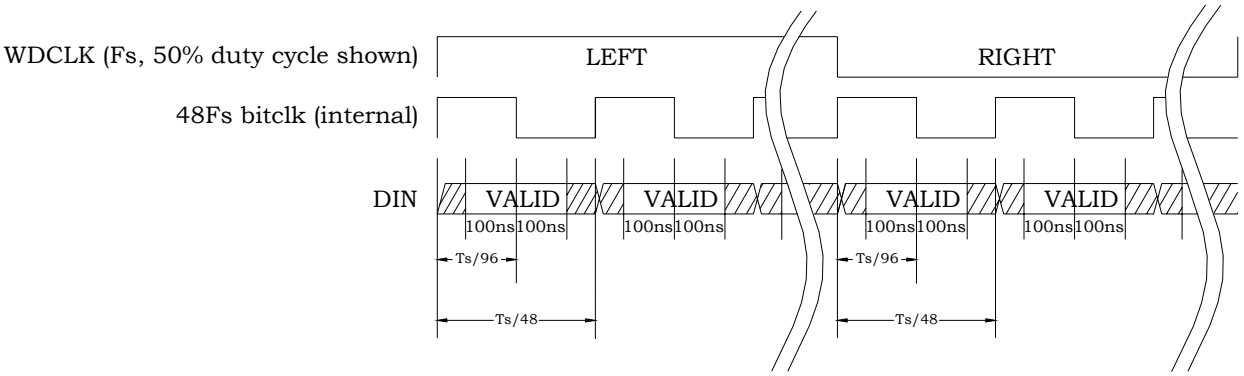


Timing Examples

32 bits/frame



24 bits/frame

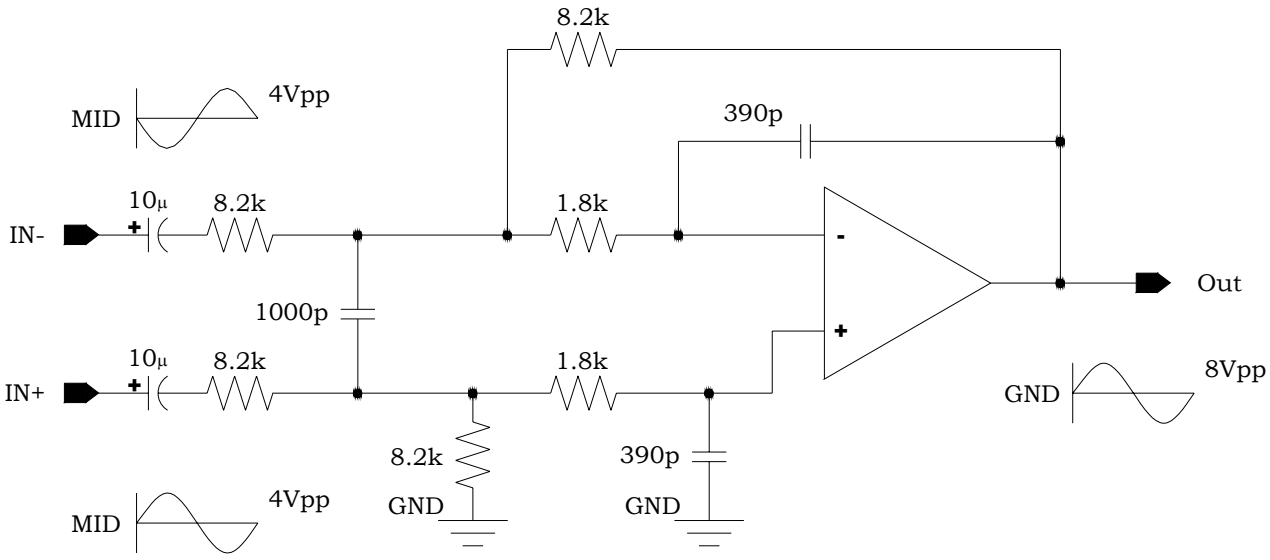


Analog Outputs

The AL1201 outputs are self-biased to the MID potential. Maximum differential output signal level is +/-4V. The outputs have been internally filtered to reduce to reduce out-of-band noise, but further filtering is suggested where this is considered critical.

Single-ended output signals

The following circuit can be used to derive a single-ended output from the AL1201. The circuit also acts as a two-pole 48kHz lowpass filter whose frequency response is flat from DC to 20kHz +/-0.3dB. Group delay deviation from flat is 1.3µs at 20kHz. High quality ceramic or film capacitors are suggested.



Differential to Single-ended Converter and 2-pole 48kHz lowpass filter

Reference and MID

The differential potential between the REF+ and REF- pins (connected to 5V and GND respectively) determines the amount of charge that is added to or removed from the modulator's first stage for each Δ-Σ modulator output (128Fs). It is very important that REF+ is well bypassed to REF- (0.1µF ceramic as close as possible to pins) to remove the unwanted effects of high frequency noise.

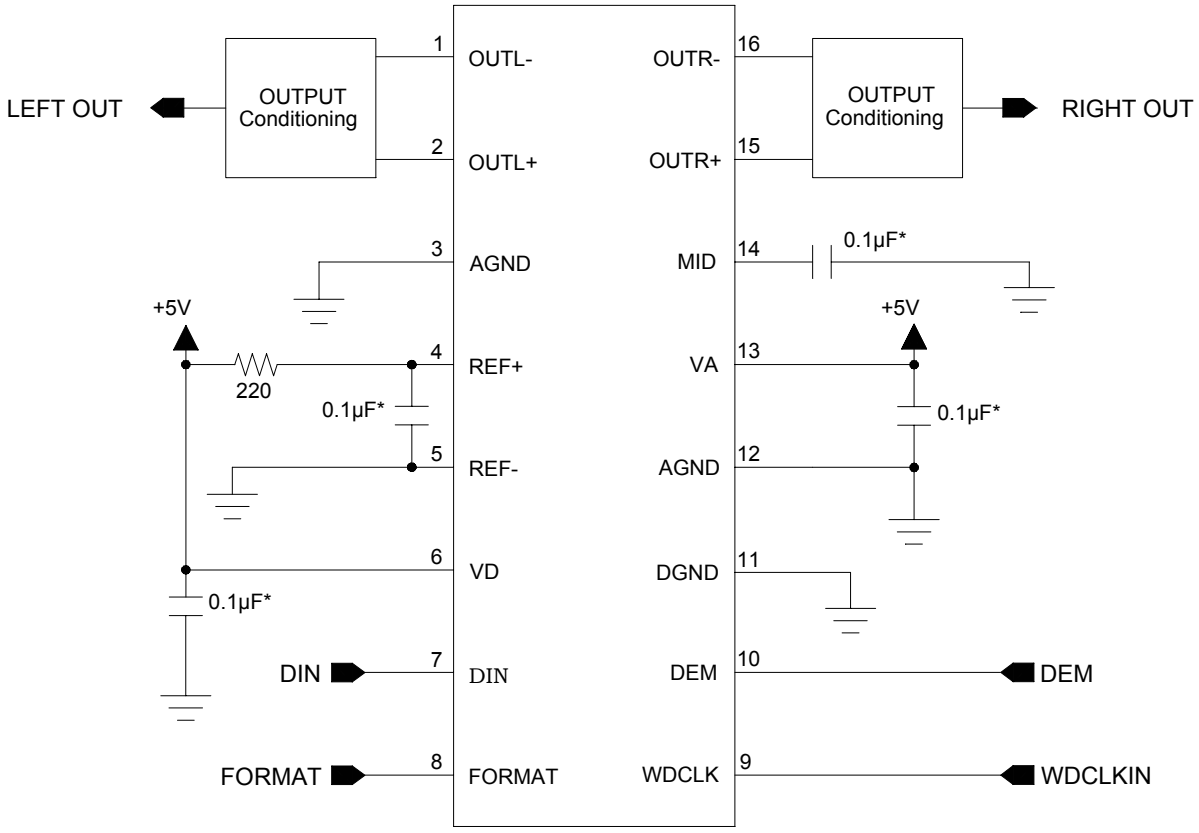
The MID potential is developed on chip (VA/2 volts) and is used to bias the internal amplifiers in the modulator and continuous-time filters. It requires a 0.1µF bypass to GND at the pin. No load current should be taken from the MID pin.

Power Supplies and Ground

A single low-impedance 5V supply is all that is required to achieve specified performance. A 5V supply plane is recommended if possible. VA and VD can be directly connected to 5V, and REF+ should be isolated with a 220 ohm resistor to 5V.

A single low impedance ground plane can be used for all GND connections, simplifying PCB layout. Each supply pin should be bypassed to GND with a 0.1µF ceramic cap positioned as close to the pins as possible.

Applications Circuit



AL1201

* Position caps as close to the pins as possible.

Suggested Connections

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Datasheet September 2003